PURIFI

PURE SOUND

Building a Straight Wire
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EVAL9
USER'S GUIDE

1 Introduction

This document describes the operation, function and usage of the EVAL9 evaluation kit ("EVM") consisting of two 1ET6525SA amplifier modules and one FE08 deluxe stereo front-end module.

1.1 Usage and Purpose

The EVM is provided for engineering evaluation and laboratory test purposes only. Great care should be taken when handling the EVM, especially when connected to power supplies and loads. Observe the voltage and power ratings and apply suitable precautions to protect the operator from electrical hazards.

Also note that the EVM is provided as an unshielded PCB assembly and should be protected from ESD as well as mechanical stress.

1.1.1 Setup and operation

1. Plug 1ET6525SA modules into the Front-End Board (FE08)
2. Place EVM on a flat surface. Note that the amplifier base plates are connected to GND and should be attached to an external heatsink, e.g., a larger aluminum plate, for extended high power testing.
3. Connect external laboratory power supplies (or other suitable PSU's) to FE08 (refer to section 4)
4. Connect audio inputs and speakers (or other suitable loads/test equipment)
   Two red LED's will light up when all supply voltages are within operational range.
5. It is recommended to disable operation (jumper) and turn off all power supplies when module is not in use

1.1.2 Power Testing

The amplifier modules are protected from overheat via individual thermal protection systems that monitor the temperature of the aluminium base plates. The aluminium plates provide limited cooling, likely adequate for full-power music as well as typical test sweeps etc., However, continuous high-power operation requires additional cooling.

2 EVAL9 Overview

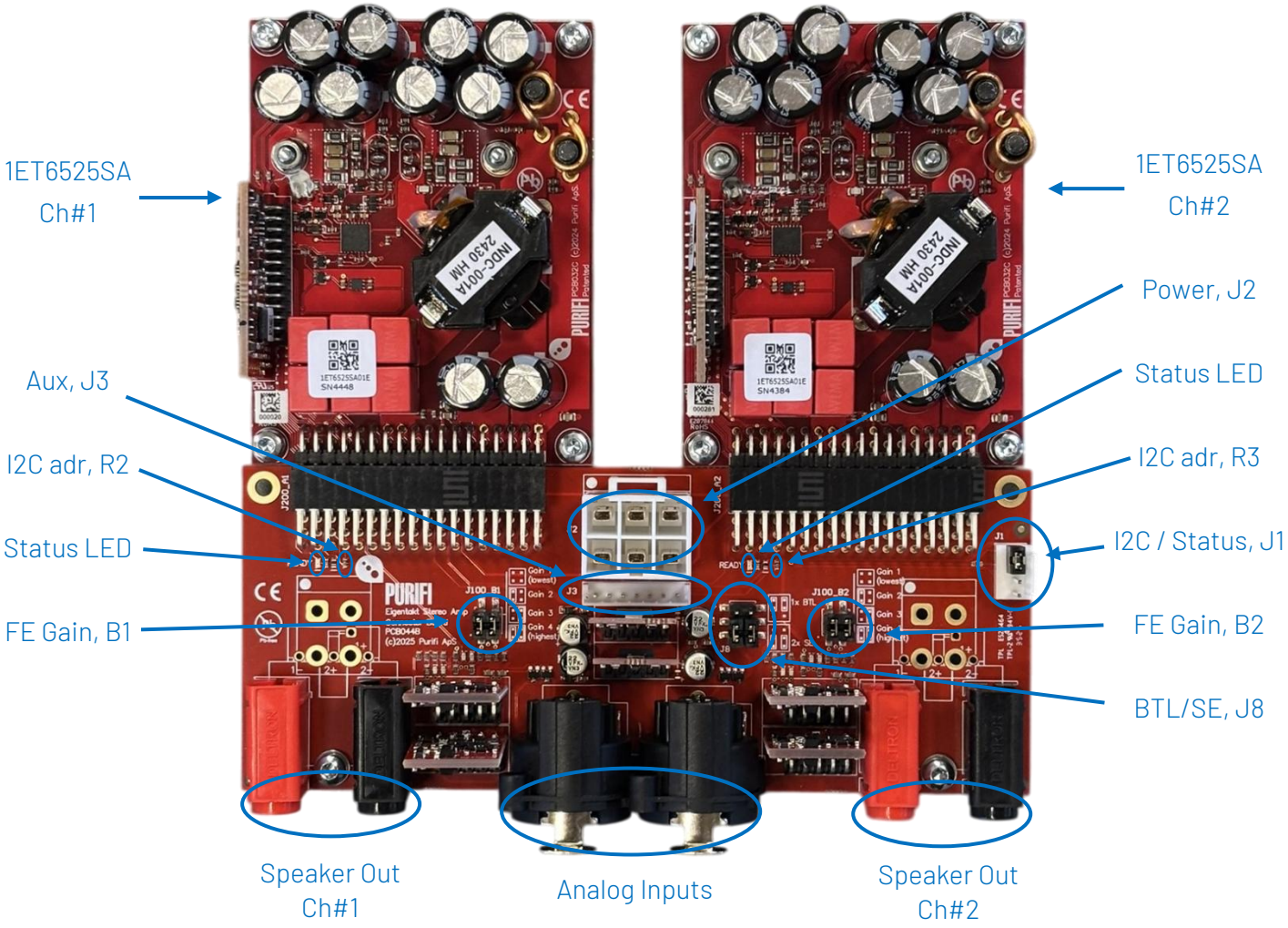


Figure 1: EVAL9 Overview

3 Interface

3.1 I2C connector, J1

Pin	Signal	Rating	I/O	Description
1	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp. HW mode is default (see section 5.2)*
2	GND		-	Ground
3	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*
4	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high

Table 1: I2C connector, J1

Note: HW mode is enabled by default. For mode configuration see section 5.1.

Connector type: Molex: 0022232042.

3.2 Power connector, J2

Pin	Signal	Rating	I/O	Description
1	VDR		P	Gate Drive Supply, referenced to -VP
2	+VP		P	Power Stage Supply, positive rail
3,6	GND		-	Ground
4,5	-VP		P	Power Stage Supply, negative rail

Table 2: Power connector, J2

Connector type equivalent: JST: B06P-VL.
Matching cable part: JST: VLP-06V.

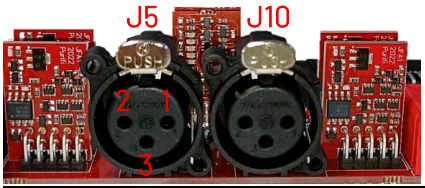
3.3 Aux connector, J3

Pin	Signal	Rating	I/O	Description
1	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
2	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high
3	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*
4	+VSBY		P	5V feed-through from external PSU
5	+VUNREG		P	Voltage regulator input, positive rail
6	GND		-	Ground
7	-VUNREG		P	Voltage regulator input, negative rail

Table 3: Aux connector, J3

Connector type: JST: B7B-EH-A(LF)(SN).
Matching cable part: JST: EHR-7.

3.4 Analog input XLR connectors, J5 & J10



Pin	Signal	Rating	I/O	Description
1	GND		-	Ground
2	IN+		I	Analog input, positive
3	IN-		I	Analog input, negative

Table 4: Analog input XLR connectors, J5 & J10

Connector type: Neutrik NC3FAAH2.

If a single-ended input is required, connect GND and IN- to the negative analog input. It is recommended to make this connection at the source end.

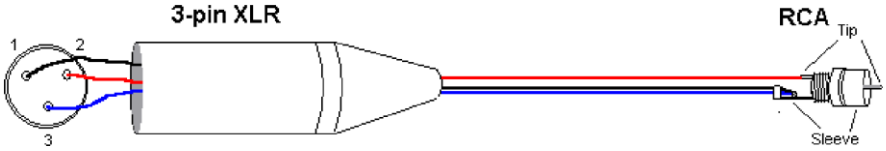
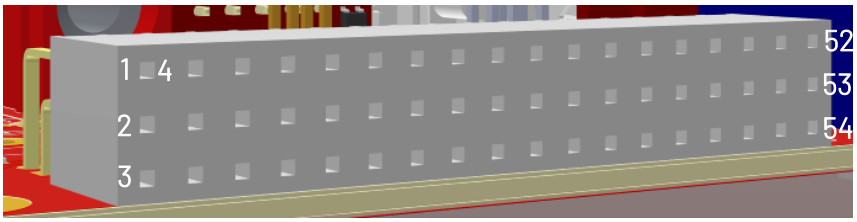


Figure 2: XLR to RCA wiring

3.5 Edge connectors, J200_A1 & J200_A2



Pin	Signal	Rating	I/O	Description
Power Supplies				
1,2, 3, 4, 7	+VP		P	Power Stage Supply, positive rail
5, 6, 8, 9, 11, 12, 37, 40, 41, 43, 46, 49, 52	GND		-	Ground
10, 13, 14, 15, 16	-VP		P	Power Stage Supply, negative rail
17	VDR		P	Gate Drive Supply, referenced to -VP
18	+VSBY		P	(optional use) External Voltage supply to amplifier module's 5V regulator
38	GND		-	Ground
39	-VOP		P	OPAMPs, negative rail
17	+VOP		P	OPAMPs, positive rail
I/O's				
19, 20, 21, 22, 23, 24, 25, 26, 27	OUT-		O	Speaker Output, negative (internally connected to GND)
28, 29, 30, 31, 32, 33, 34, 35, 36	OUT+		O	Speaker Output, positive
42, 50, 51	NC		-	Not connected
44	IN+		I	Analog Input, positive
45	IN-		I	Analog Input, negative
47	HS/ADDR		I	Mode/I2C Address Selection; set by one 1% resistor.
48	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
53	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high
54	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*

Table 5: Edge Connectors, J200_A1 & J200_A23

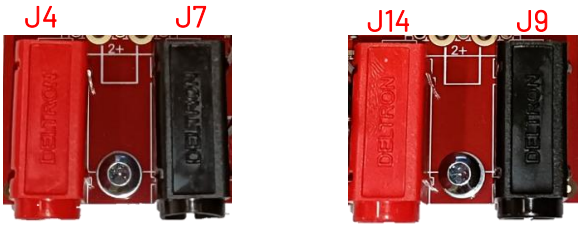
Connector type: Samtec: SSW-118-02-T-T-RA

1 +VP	4 +VP	7 +VP	10 -VP	13 -VP	16 -VP	19 OUT-	22 OUT-	25 OUT-	28 OUT+	31 OUT+	34 OUT+	37 GND	40 GND	43 GND	46 GND	49 GND	52 GND
2 +VP	5 GND	8 GND	11 GND	14 -VP	17 VDR	20 OUT-	23 OUT-	26 OUT-	29 OUT+	32 OUT+	35 OUT+	38 -VOP	41 GND	44 IN+	47 ADDR	50 NC	53 SDA
3 +VP	6 GND	9 GND	12 GND	15 -VP	18 +VSBY	21 OUT-	24 OUT-	27 OUT-	30 OUT+	33 OUT+	36 OUT+	39 +VOP	42 NC	45 IN-	48 /AMPON	51 NC	54 SCL

Figure 3: Edge Connector pinout

Note: Care should be taken to only connect the 1ET6525SA to the two lowest rows of pins.

3.6 Speaker output connectors, J4, J7, J14 & J9



Pin	Signal	Rating	I/O	Description
J4	OUT+		O	Speaker output, positive – Channel 1
J7	OUT-		O	Speaker output, negative – Channel 1
J14	OUT+		O	Speaker output, positive – Channel 2
J9	OUT-		O	Speaker output, negative – Channel 2

Table 6: Speaker output connectors, J4, J7, J14, J9

Connector: High current banana socket: Deltron: 571-0100(Black), 571-0500(Red)

3.7 Gain-select jumpers, J100_B1 & J100_B2

FE08 includes a pre-gain stage with four selectable settings. The gain can be set by placing jumpers as shown below:

Description	Gain 1 (lowest)	Gain 2	Gain 3	Gain 4 (highest)
Front-End gain	3 dB	11.6 dB	13.7 dB	17.2 dB
Total EVM gain	15.3 dB	23.9 dB	26.0 dB	29.5 dB
Jumper setting				

Table 7: Gain jumpers, B1 & B2

The pre-gain stage uses PURIFI's discrete op-amp **JFA1**, configured as balanced/single-ended to balanced gain stage as shown below:

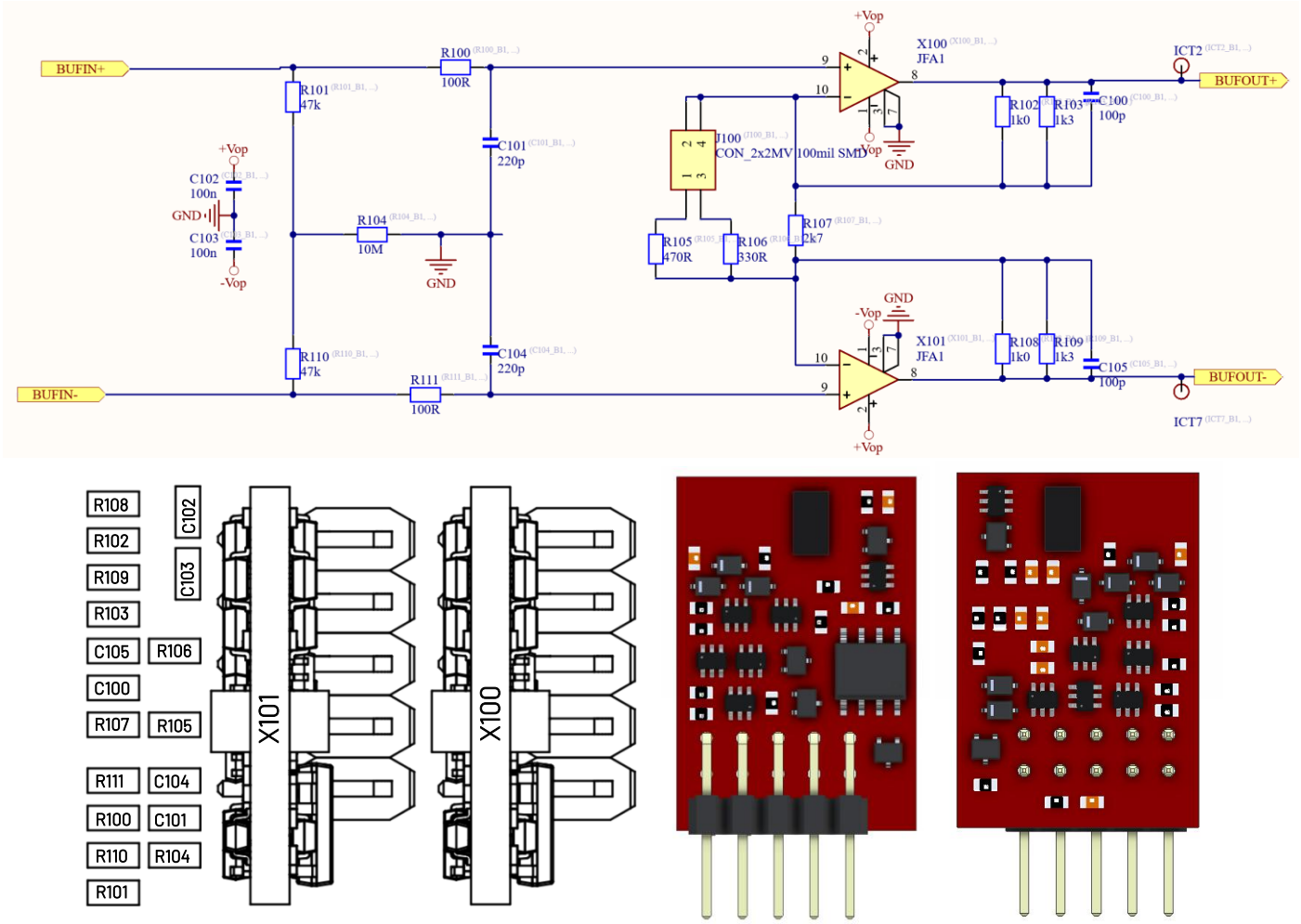
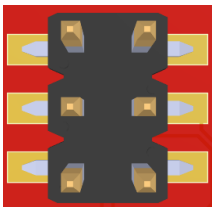


Figure 4: Buffer schematic

Differential input impedance is 94.0 kohm.

3.8 BTL/SE jumper, J8



FE08 supports 1x BTL (bridged) or 2x SE (single-ended) operation. The mode can be chosen by placing the jumpers as shown below.

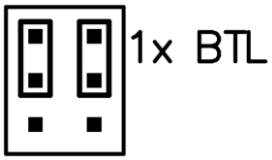
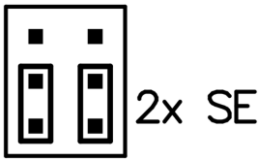
Description	1x BTL	2x SE
Jumper setting		

Table 8: BTL/SE jumper, J8

Connector J5 serves as the input for BTL operation. In this mode, the amplifier outputs CH1 (+) and CH2 (–) are used to drive a single load. This configuration provides 2x higher output voltage swing and 4x increased power compared to single-ended mode. Note in BTL mode nominal load changes to 8ohm, and it will be current limited in 4ohm load.

Connect the speaker only between CH1 (+) and CH2 (–) as shown below.

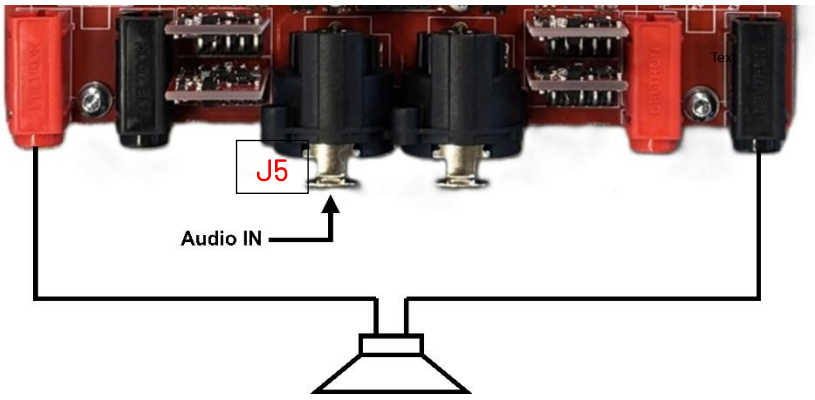


Figure 5: BTL output configuration

WARNING - BTL mode: High voltage of up to 130V between CH1 (+) and CH2 (–).
Do not touch these terminals.

4 Power Supplies

The figure below shows the required power supplies and how to connect these to FE08:

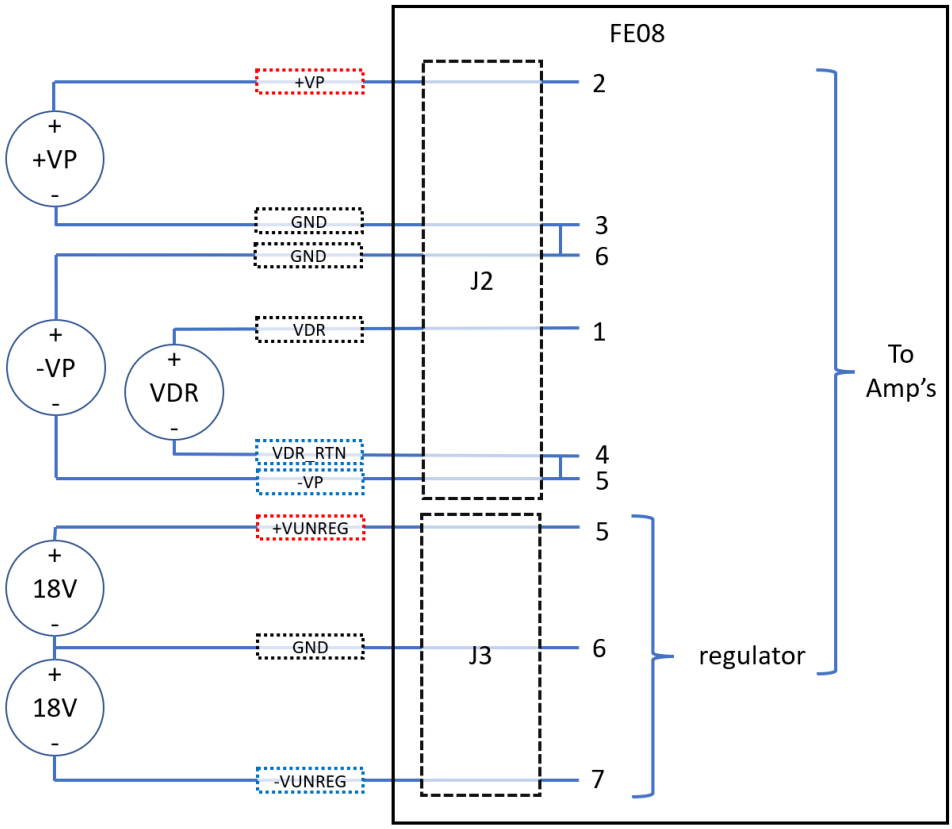


Figure 6: Power Supplies

All supplies levels should be cross-checked with the Recommended Operation Conditions as specified in the respective amplifier module data sheet.

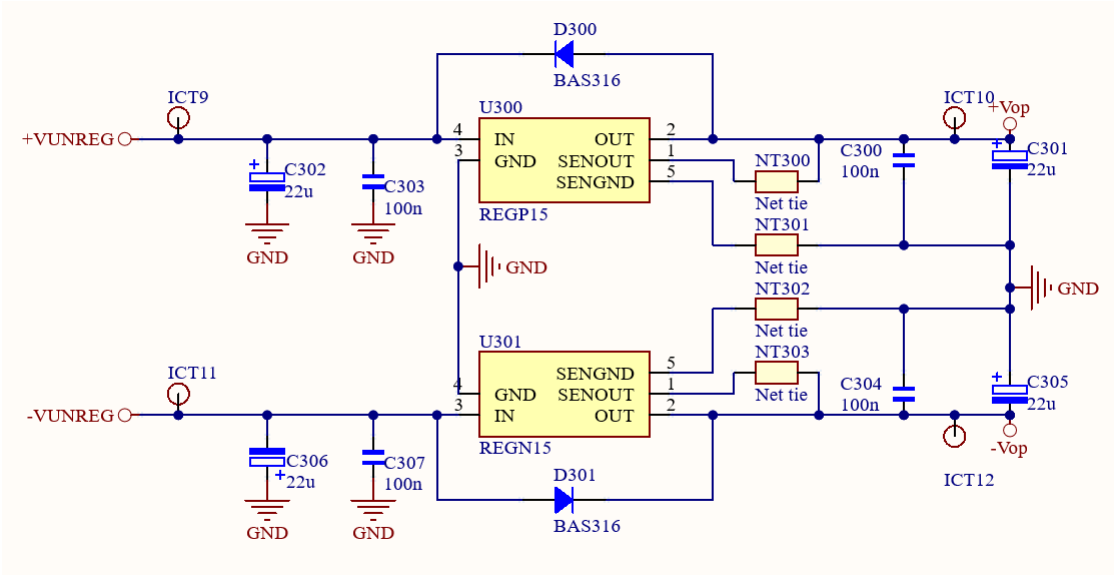
Recommended supply voltages for EVAL9 (please also refer to the 1ET6525SA Data Sheet):

Parameter		Min	Typ	Max	Unit
Power Supplies					
+VP	Power Stage, positive rail voltage	32	65	70	V
-VP	Power Stage, negative rail voltage	-70	-65	-32	V
VDR	Gate Drive, voltage (must be referenced to -VP)	13.6	15	16.5	V
+VUNREG	OPAMPs, positive rail voltage	16.4	18	25	V
-VUNREG	OPAMPs, negative rail voltage	-25	-18	-16.4	V

Table 9: Recommended Supply Voltages

4.1 Linear Regulators

FE08 includes two low-noise, low-impedance discrete linear regulators for the OPAMP's negative and positive supply voltages, +Vop & -Vop. The schematic is shown here below:



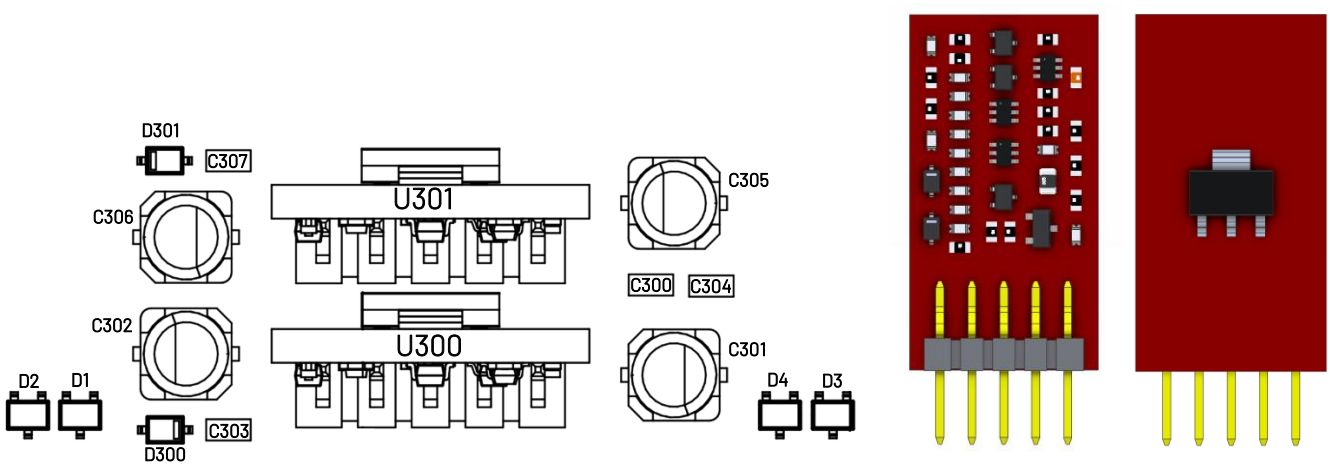


Figure 7: Linear Regulator Schematic

5 Operating Modes & Status Reporting

5.1 Mode Configuration

The EVAL9 can operate in two modes:

1. HW Mode: all control and status via pins (HW interface) – DEFAULT CONFIGUTATION
2. SW Mode: enables control and status via I2C interface

FE08 is configured for HW Mode by default. To reconfigure for SW Mode, at bit of soldering is required, see Table 10 and Figure 8:

FP	Channel	Description	HW Mode	SW Mode
R202_A1	1	Mode Selection	**Diode**	0Ω shunt
R202_A2	2			
R2	1	I2C Address Selection	**Open**	Refer to data sheet
R3	2			

Table 10 Mode Selection

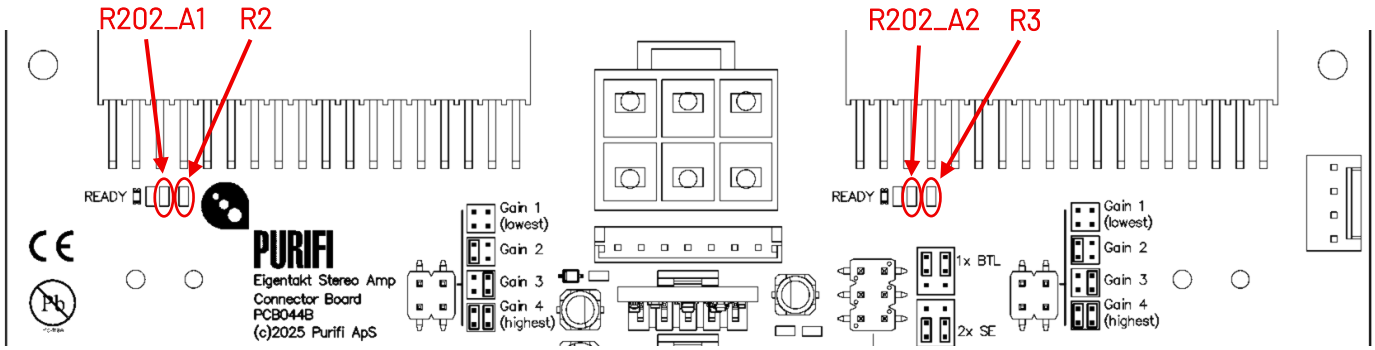


Figure 8: Mode Selection

5.2 HW Mode

The amplifier modules are controlled via J3 which is connected to amplifier control signal /AMPON. /AMPON is also made available on connector J1 and can be controlled via external source.

Amplifier status is signaled via READY and /FATAL:

READY signals are connected to individual LED's on FE08.

/FATAL signals are wire OR'ed together on FE08 and pinned out on connectors: J1 and J3.

5.3 SW Model

The main feature of the SW Mode is access via I2C to status and control information. The I2C register map can be found in the amplifier data sheet.

I2C is accessed via SCL, SDA on connectors J1 and J3.

The I2C address can be programmed via value of resistors R2 and R3 on FE08. Refer to the **Mode Selection via HS/ADR** table in the amplifier data sheet for information on resistor value vs. I2C address.

6 Mechanical Specifications & System Considerations

6.1 EVAL9 Dimensions

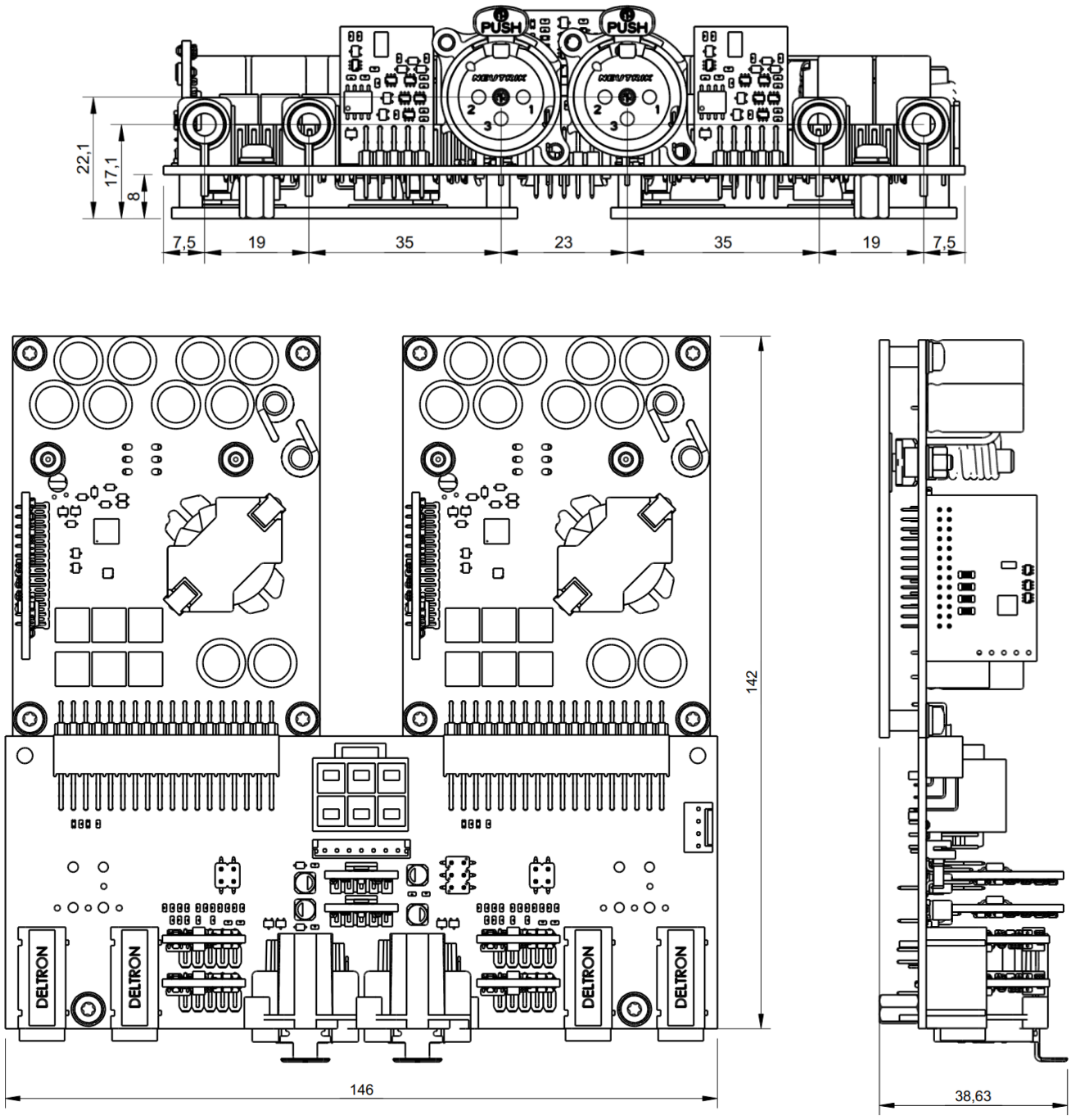


Figure 9: Dimensions

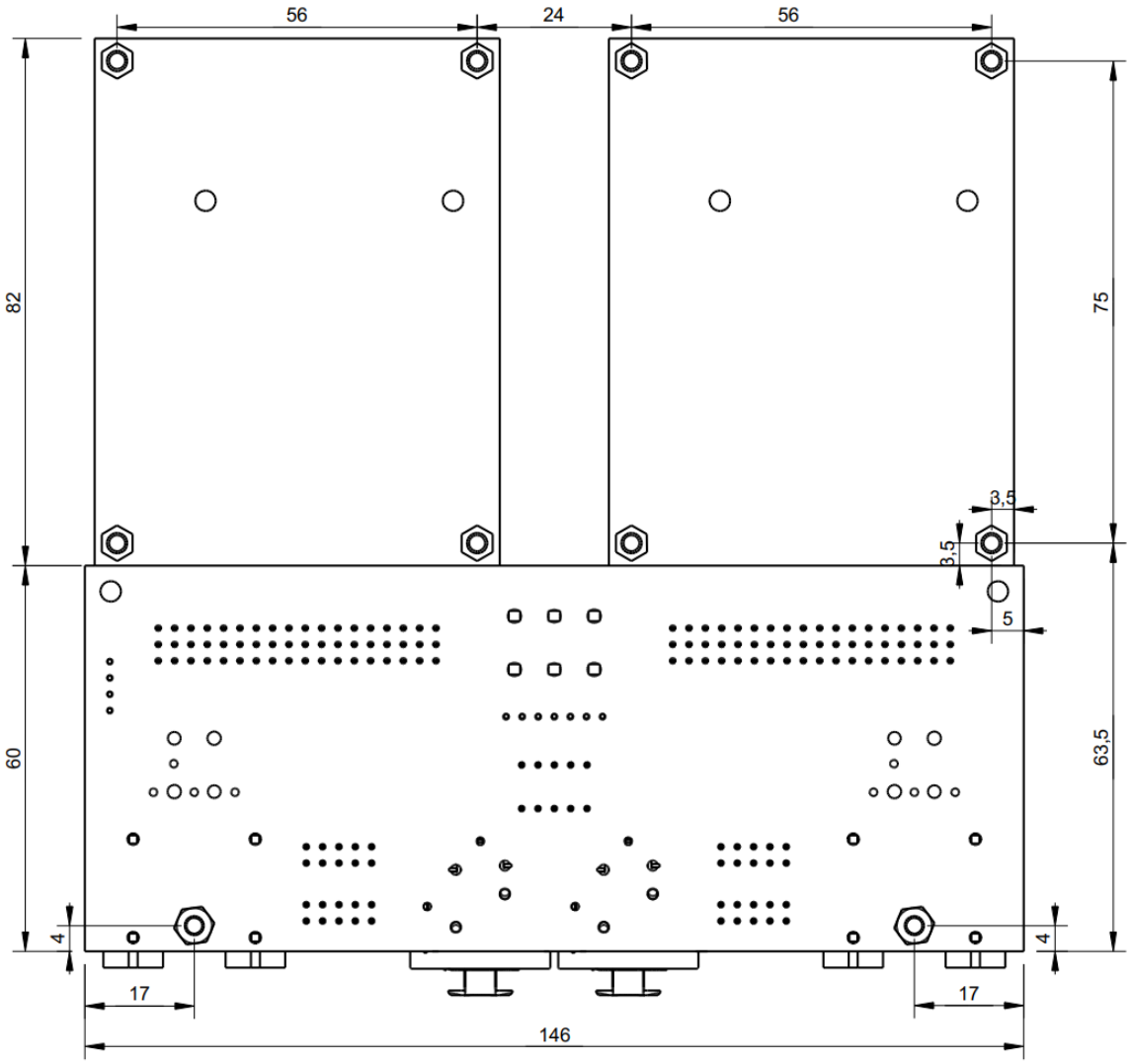


Figure 10: Bottom-side mounting holes

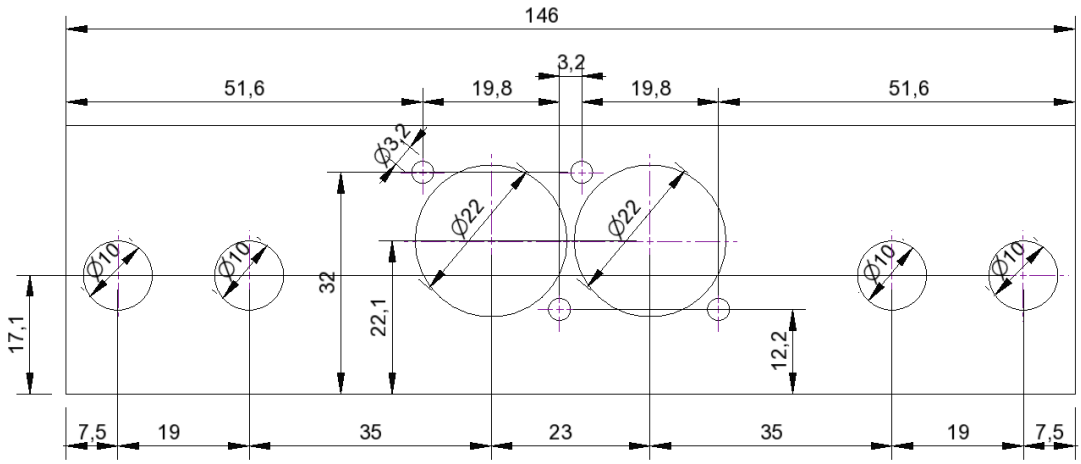


Figure 11: Back plate mounting holes

Note: Dimensions from bottom mounting plate include the 8mm standoff.

6.2 Thermal Requirements

While 1ET6525SA has very low idle losses and high overall efficiency, adequate cooling is essential for sustained power delivery. Careful consideration must be given to design the thermal system to achieve desired power specifications.

It is recommended to mount the module on a heatsink, e.g., an adequately designed aluminum chassis.

6.3 Mechanical Requirements

Related to mechanical robustness of the end application: It is the reasonability of the system integrator to specify process, materials, locations, etc. for e.g., gluing of critical components which may be required and to prove/document short- and long-term performance and reliability. The system integrator must ensure integrity of mounting methods and materials used related to fixation of the module. It is recommended to thoroughly test the final product for robustness against, e.g., shock and vibration.

6.4 Compliance Testing

1ET6525SA is designed with considerations for compliance of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required.

7 External Standby Switch

Standby is controlled by the /AMPON signal, which is available on J1 pin 1. J1 also includes a GND pin, allowing an external standby switch to be implemented by connecting a switch between pin 1 and pin 2 and removing the jumper from J1.

The FE08 board, in HW mode, includes two diodes that OR the READY signals from Ch1 and Ch2. An ON/OFF indicator can therefore be implemented by connecting an LED with a 680-ohm resistor between J1 pin 4 and J1 pin 2.

A wiring diagram example is shown below:

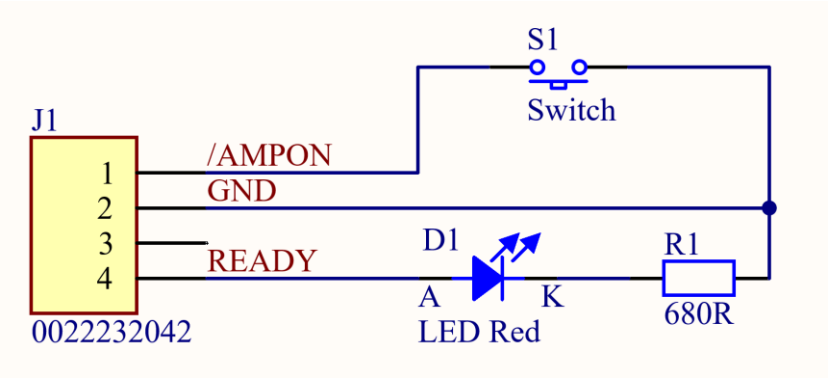


Figure 12: External Standby Switch

8 Revision History

Rev	Date	Description	ID
(1.00)	2025-10-31	Initial Issue	AJA
(1.10)	2025-11-19	Updated image and orientation for AUX Connector, J3	AJA

Table 11: Revision History

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1.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS. 1.2 User must read and apply the user guide and other available documentation provided by PURIFI ApS regarding the EVM prior to handling or using the EVM. 1.3 Safety-Related Warnings and Restrictions: 1.3.1 User shall operate the EVM within PURIFI ApS's recommended specifications and environmental considerations stated in the specification or other available documentation provided by PURIFI APS, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM documentation prior to connecting any load to the EVM output. During normal operation, even with the inputs and outputs are kept within the specified allowable ranges, some circuit components may have elevated case temperatures. When working with the EVM, please be aware that the EVM may become very warm. If there is uncertainty as to the ratings and specifications, please contact PURIFI ApS prior to connecting interface electronics including input power and intended loads. 1.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees. 1.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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