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EVAL7
USER'S GUIDE

1 Introduction

This document describes the operation, function and usage of the EVAL7 evaluation kit ("EVM") consisting of one 1ET6525SA amplifier module and one FE03 front-end module.

1.1 Usage and Purpose

The EVM is provided for engineering evaluation and laboratory test purposes only. Great care should be taken when handling the EVM, especially when connected to power supplies and loads. Observe the voltage and power ratings and apply suitable precautions to protect the operator from electrical hazards.

Also note that the EVM is provided as an unshielded PCB assembly and should be protected from ESD as well as mechanical stress.

1.1.1 Setup and operation

1. Plug 1ET6525SA module into the Front-End Board (FE03)
2. Place EVM on a flat surface Note that the amplifier base plate is connected to GND and should be attached to an external heatsink, e.g., a larger aluminum plate, for extended high power testing.
3. Connect external laboratory supplies (or other suitable PSU's) to FE03 (refer to section 4)
4. Connect audio input and speaker (or other suitable load/test equipment)
5. Enable operation via toggle-switch on FE03
   A red LED will light up when all supply voltages are within operational range.
6. It is recommended to disable operation (toggle-switch) and turn off all power supplies when module is not in use

1.1.2 Power Testing

The amplifier module is protected from overheat via thermal protection system that monitors the temperature of the aluminium base plate. The aluminium plate provides limited cooling, likely adequate for full-power music as well as for typical test sweeps etc., However, for continuous high power delivery additional cooling is required.

2 EVAL7 Overview

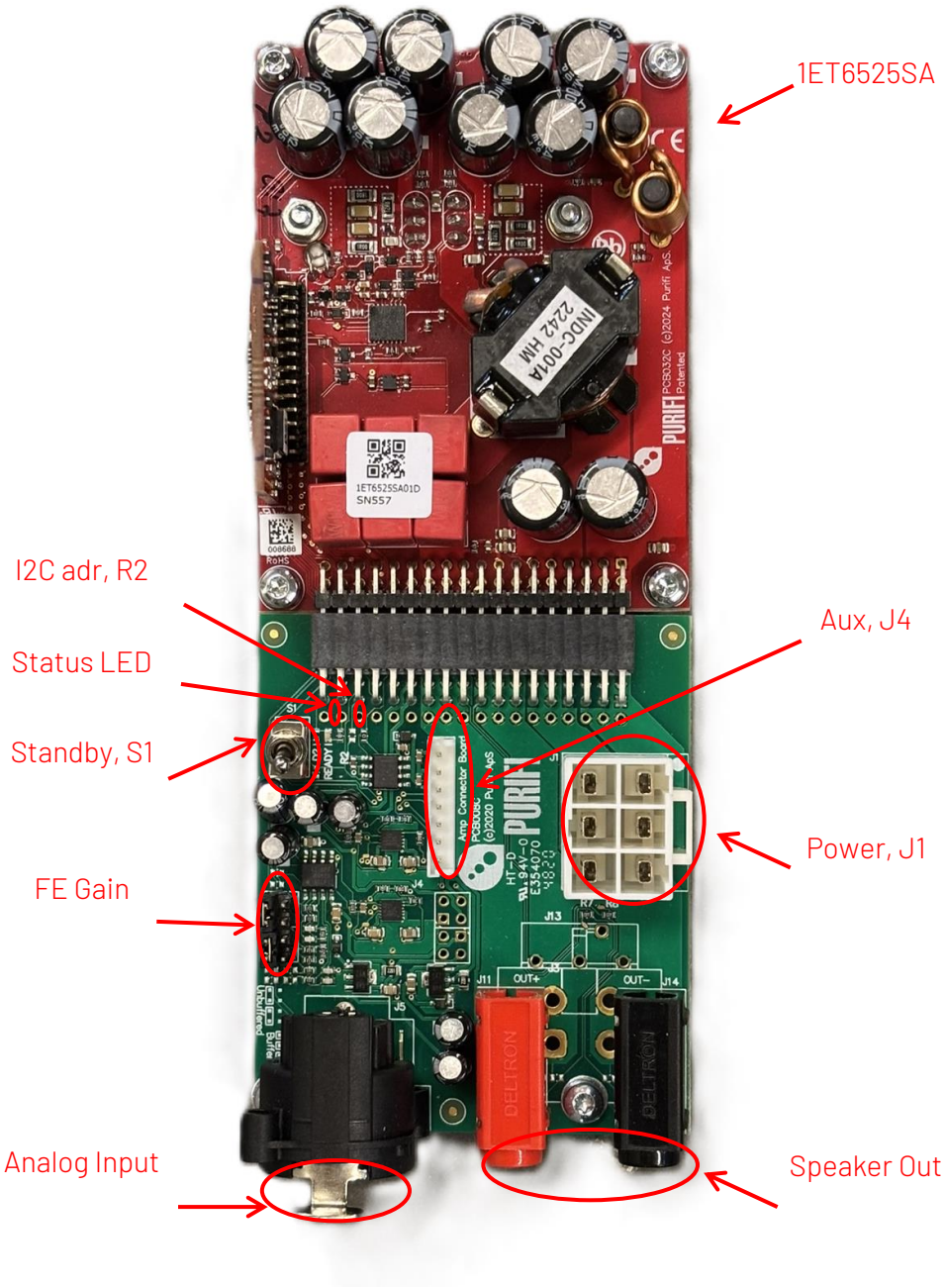


Figure 1 EVAL7 Overview

3 Interface

3.1 Standby switch, S1

Position	Description
Towards 1ET6525SA	Operational – Power stage is on
Away from 1ET6525SA	Standby, Power stage is off

Table 1 Standby switch, S1

3.2 Power connector, J1

Pin	Signal	Rating	I/O	Description
1	VDR		P	Gate Drive Supply, referenced to -VP
2	+VP		P	Power Stage Supply, positive rail
3,6	GND		P	Ground
4,5	-VP		P	Power Stage Supply, negative rail

Table 2 Power connector, J1

Connector type equivalent: JST: B06P-VL.
Matching cable part: JST: VLP-06V.

3.3 Aux connector, J4

Pin	Signal	Rating	I/O	Description
1	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
2	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high
3	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*
4	+5V		P	5V output (from onboard regulator), 20mA max load. Requires R1 mounted
5	+VUNREG		P	Voltage regulator input, positive rail
6	GND		P	Ground
7	-VUNREG		P	Voltage regulator input, negative rail

Table 3 Aux connector, J3

Connector type: JST: B7B-EH-A(LF)(SN).
Matching cable part: JST: EHR-7.

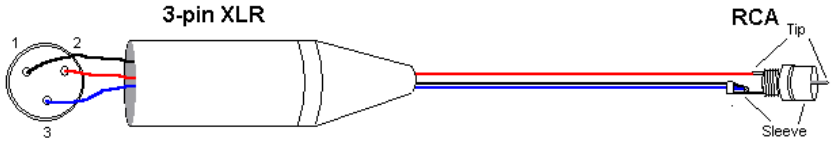
3.4 Analog input XLR connector, J5

Pin	Signal	Rating	I/O	Description
1	GND		-	Ground
2	IN+		I	Analog input, positive
3	IN-		I	Analog input, negative

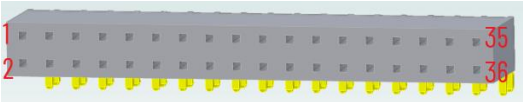
Table 4 Analog input XLR connector, J5

Connector type: Neutrik NC3FAH2

If a single ended input is need then connect GND and IN- to the negative analog input. When using the FE03 gain stage the single ended input is converted to a fully balanced signal and then fed to the 1ET6525SA module. The connection of the GND and IN- is best done at the source end.



3.5 Edge connector, J10

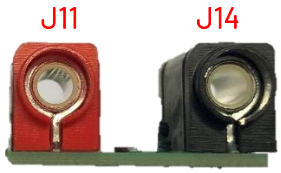


Pin	Signal	Rating	I/O	Description
Power Supplies				
1, 2	+VP		P	Power Stage Supply, positive rail
3,4,5 6,7,8	GND		P	Ground
9,10	-VP		P	Power Stage Supply, negative rail
11	VDR		P	Gate Drive Supply, referenced to -VP
12	VD		P	(option use) External Voltage supply to on-board 5V regulator
26	+VOP		P	OPAMPs, positive rail
25	-VOP		P	OPAMPs, negative rail
27	GND		P	Ground
I/O's				
13,14,15, 16,18	OUT-		O	Speaker Output, negative (internally connected to GND)
20,21,22, 23,24	OUT+		O	Speaker Output, positive
17, 19, 28,33,34	NC		-	Not connected
29	IN+		I	Analog Input, positive
30	IN-		I	Analog Input, negative
31	HS/ADDR		I	Mode/I2C Address Selection; set by one 1% resistor.
32	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
35	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high
36	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*

Table 5 Edge Connector, J10

Connector type: Samtec: SSW-118-02-T-D-RA

3.6 Speaker output connectors, J11 & J14



Pin	Signal	Rating	I/O	Description
J11_A1	OUT+		O	Speaker output, positive – RED
J13_A1	OUT-		O	Speaker output, negative – BLACK

Table 6 Speaker output connectors, J11 & J14

Connector: 4mm banana socket: Deltron: 571-0100(Black), 571-0500(Red)

The FE03 has three speaker connection options:

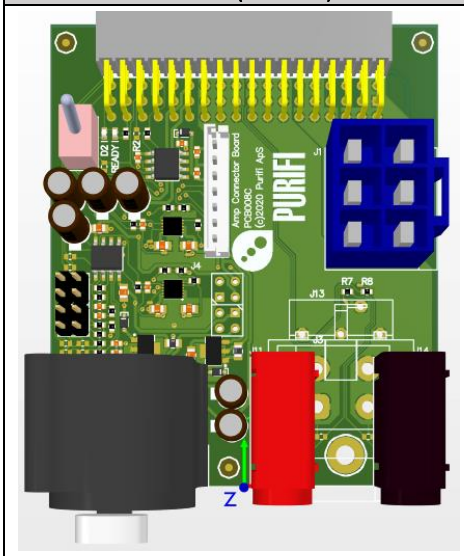
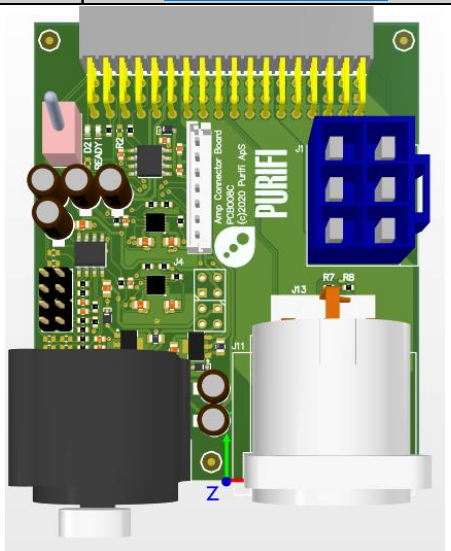
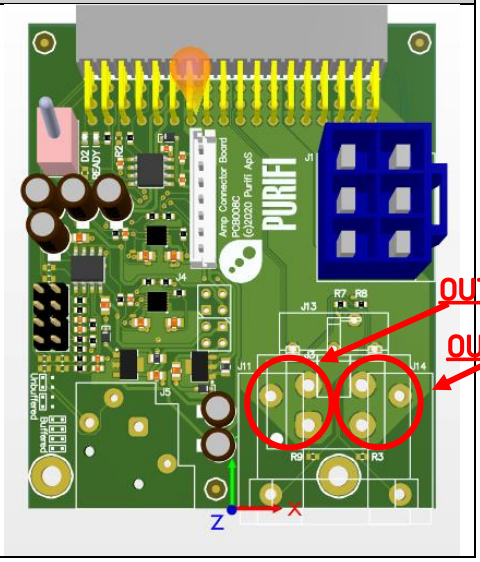
Banana (default)	Speakon (Neutrik NL4MDH3)	No Connector – for ext wire
		

Table 7 Speaker output connector options

Note: For use with a speaker output connector external to the FE03 PCB, the connector's terminals should each be connected with wires soldered to one or more of the holes indicated above.

3.7 Gain/Bypass jumpers, J15 & J16

FE03 includes a ~13dB pre-gain stage for a total EVM gain of ~26dB. The pre-gain stage can be bypassed by location of two sets of jumpers:

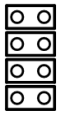
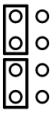
Description	Pre-gain enabled	Pre-gain bypassed
Front-End gain	~14dB	0dB
Total EVM gain	~27dB	~13dB
Jumper setting		

Table 8 Gain/Bypass jumpers, J15 & J16

The pre-gain stage is made with a dual OPA1612 configured as Balanced/single-ended to balanced gain stage as shown below:

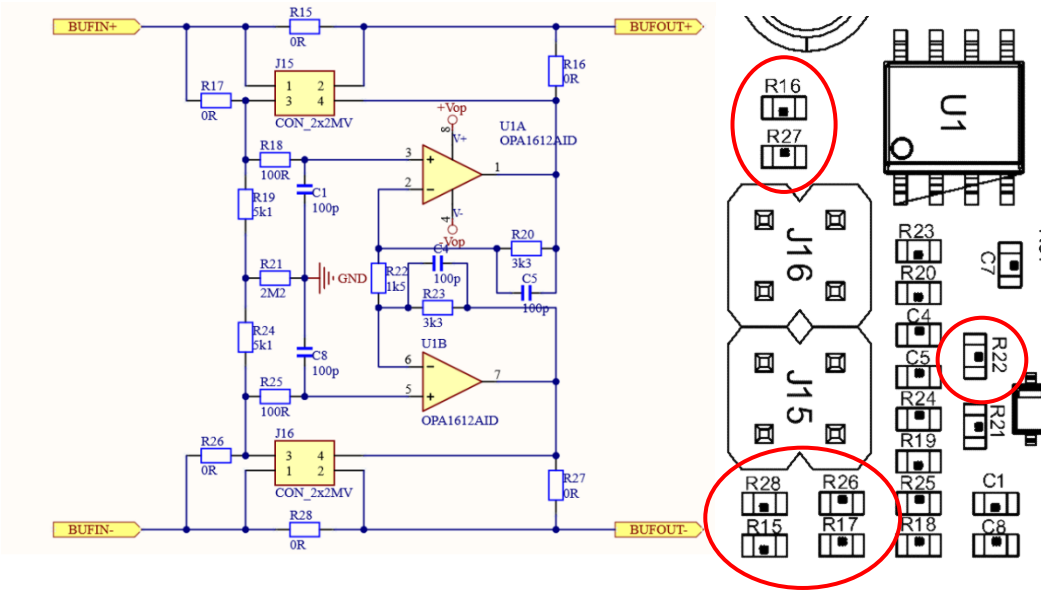


Figure 2 Buffer Schematic

Differential input impedance is 10.2kohm

The 0R resistors: R15, R16, R17, R26, R27, R28 are not mounted per default
The gain stage can be enabled/by-passed with the help of pin headed J15/J16 and jumpers as shown in Table 8.
If a fixed setting is needed the 0R resistors can be used as follows:

Description	Pre-gain enabled	Pre-gain bypassed
Front-End gain	~14dB	0dB
Total EVM gain	~27dB	~13dB
Resistors mounted	R16, R17, R26, R27	R15, R28
Resistors NOT mounted	R15, R28	R16, R17, R26, R27
Input Impedance	10.2kohm	2.2kohm

Table 9 Gain/Bypass resistors, B1 & B2

If a different gain is needed resistor R22 can be modified.
Gain = 1+(R20+R23)/R22 = 1+(3.3K+3.3k)/1.5K = 5.4 = 14.6dB

4 Power Supplies

Refer to below figure showing required power supplies and how to connect these to FE03:

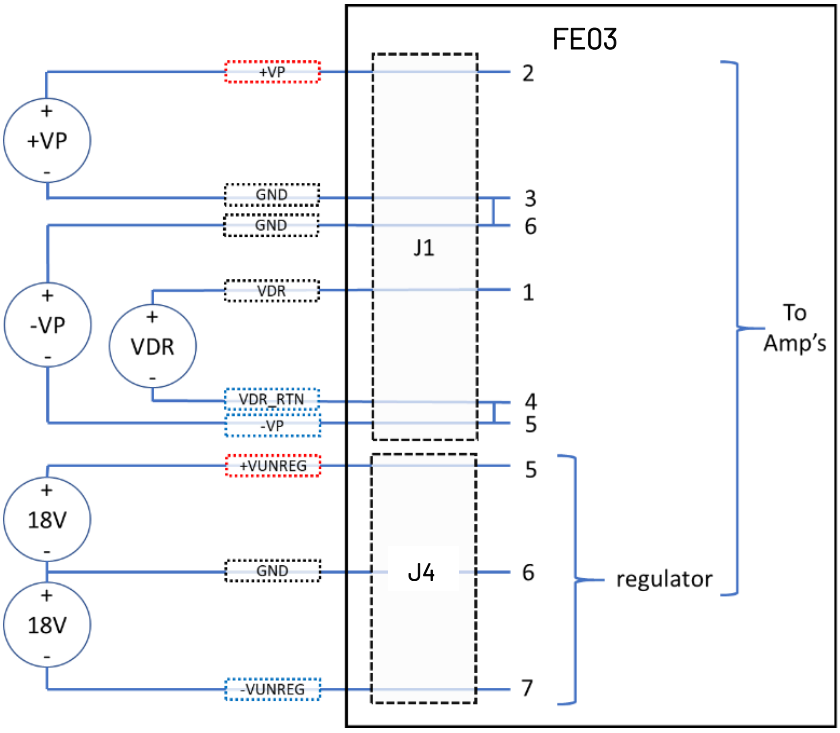


Figure 3 Power Supplies

All supply levels should be crosschecked with the Recommended Operation Conditions as specified in the respective amplifier module data sheet.

Recommended supply voltages for EVAL7 (please also refer to the 1ET6525SA Data Sheet):

Parameter		Min	Typ	Max	Unit
Power Supplies					
+VP	Power Stage, positive rail voltage	32	65	70	V
-VP	Power Stage, negative rail voltage	-70	-65	-32	V
VDR	Gate Drive, voltage (must be referenced to -VP)	13.6	15	16.5	V
+VUNREG	OPAMPs, positive rail voltage	14.5	15	25	V
-VUNREG	OPAMPs, negative rail voltage	-25	-15	-14.5	V

Table 10 Recommended Supply Voltages

4.1 Linear Regulators

FE03 includes two low noise voltage regulators for the OPAMP's negative and positive supply voltages (+VOP and -VOP) and a 5V regulator for the standby regulator (+VSBY).

5 Operating Modes & Status Reporting

5.1 Mode Configuration

The EVAL7 can operate in two modes:

1. HW Mode: all control and status via pins (HW interface) – DEFAULT CONFIGUTATION
2. SW Mode: enables control and status via I2C interface

FE03 is configured for HW Mode by default. To reconfigure for SW Mode, at bit of soldering is required, see Table 11 and Figure 4:

FP	Channel	Description	HW Mode	SW Mode
D2	1	Mode Selection	**Diode**	0Ω shunt
R2	1	I2C Address Selection	**open**	Refer to 1ET6525SA data sheet

Table 11 Mode Selection

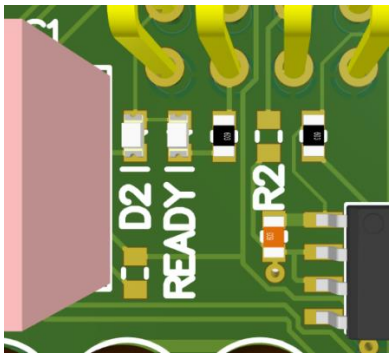


Figure 4 Mode Selection

5.2 HW Mode

The amplifier modules are controlled via toggle switch S1 connected to amplifier control signal /AMPON. /AMPON is also made available on connectors J4 and can be controlled via external source.

Amplifier status is signaled via READY and /FATAL:

READY signal is connected to a RED LED on FE03, and is pinned out on connector J4
/FATAL signal is pinned out on connector: J4.

5.3 SW Model

The main feature of the SW Mode is access via I2C to status and control information. The I2C register map can be found in the amplifier data sheet.

I2C is accessed via SCL, SDA on connectors J2, J3 and J16.

The I2C address can be programmed via value of resistors R2 and R5 on FE03. Refer to the **Mode Selection via HS/ADR** table in the amplifier data sheet for information on resistor value vs. I2C address.

6 Mechanical Specifications & System Considerations

6.1 EVAL7 Dimensions

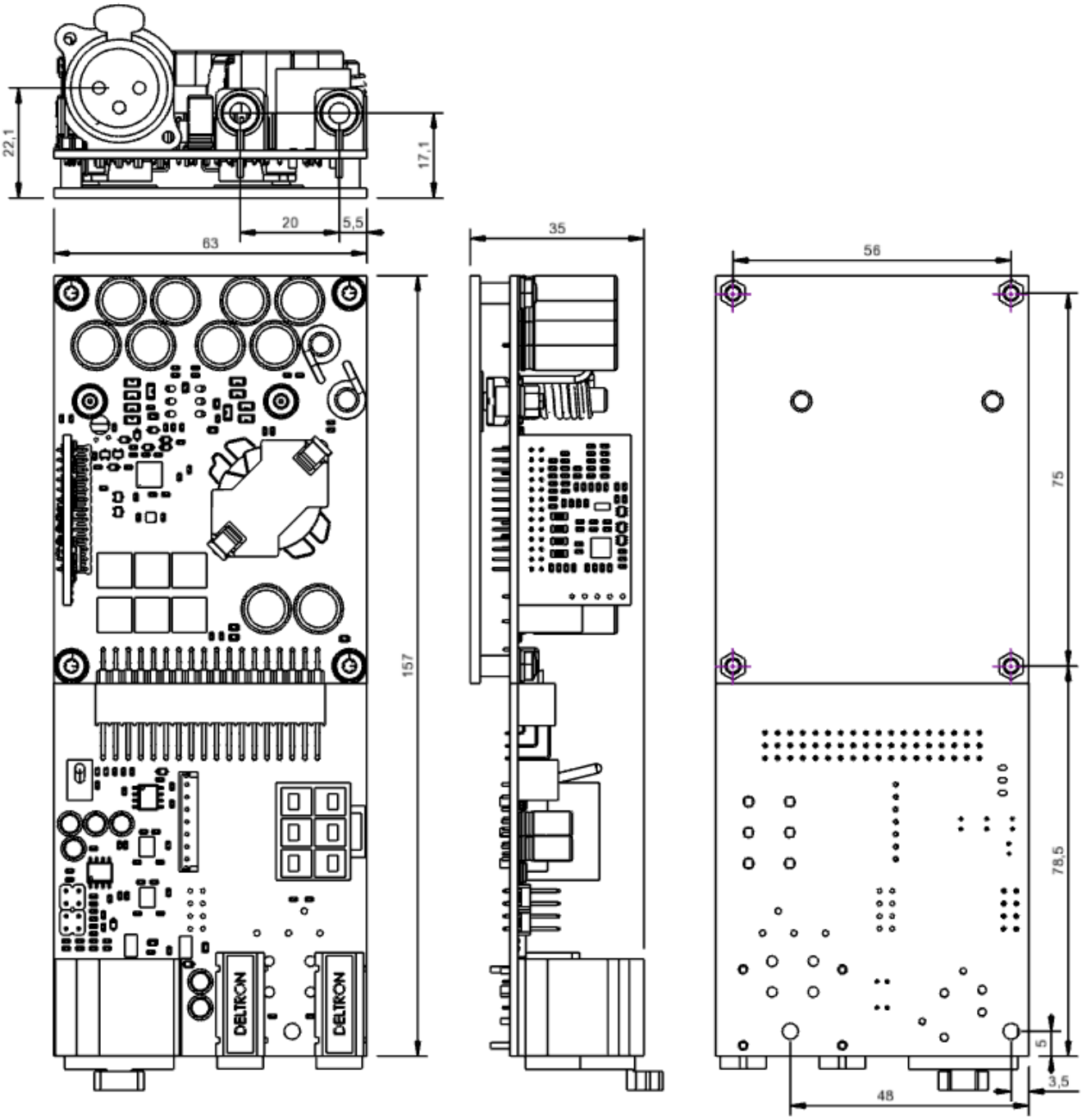


Figure 5 Dimensions

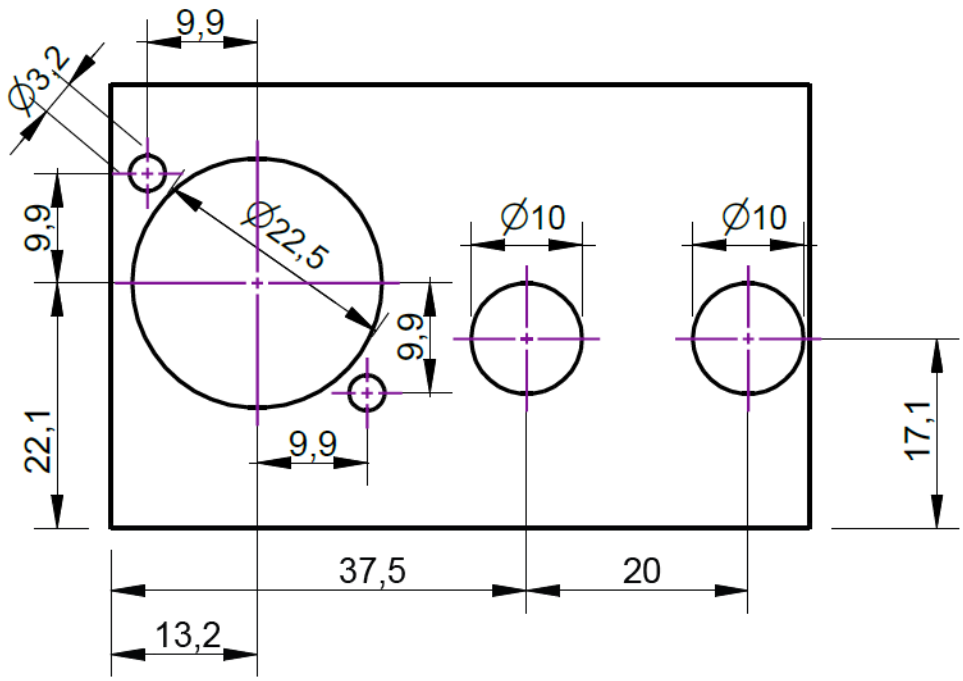


Figure 6 Back plate mounting holes

Note: Dimensions from bottom mounting plate including the 8mm standoff.

6.2 Thermal Requirements

While 1ET6525SA has very low idle losses and high overall efficiency, adequate cooling is essential for sustained power delivery. Careful considerations must be given to design the thermal system in order to achieve desired output power specifications.

It is recommended to mount the module on a heatsink, e.g., an adequately design aluminum chassis.

6.3 Mechanical Requirements

Related to mechanical robustness of the end application, it is the reasonability of the system integrator to specify process, materials, locations, etc. for e.g., gluing of critical components which may be required and to prove/document short- and long-term performance and reliability. The system integrator must ensure integrity of mounting method and materials used related to fixation of the module. It is recommended to thoroughly test the final product for robustness against, e.g., shock and vibration.

6.4 Compliance Testing

1ET6525SA is designed with considerations for compliance of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required.

7 External Standby Switch

Standby is controlled by the /AMPON signal, that is present on J4,p1.

J4 also have a GND pin, so an external standby switch can be implemented by wiring a switch on J3,p1 to J3,p6.

The FE03 default mode setting is 'HW-mode'.

A diode and on/off switch can be implemented as shown below (red box).

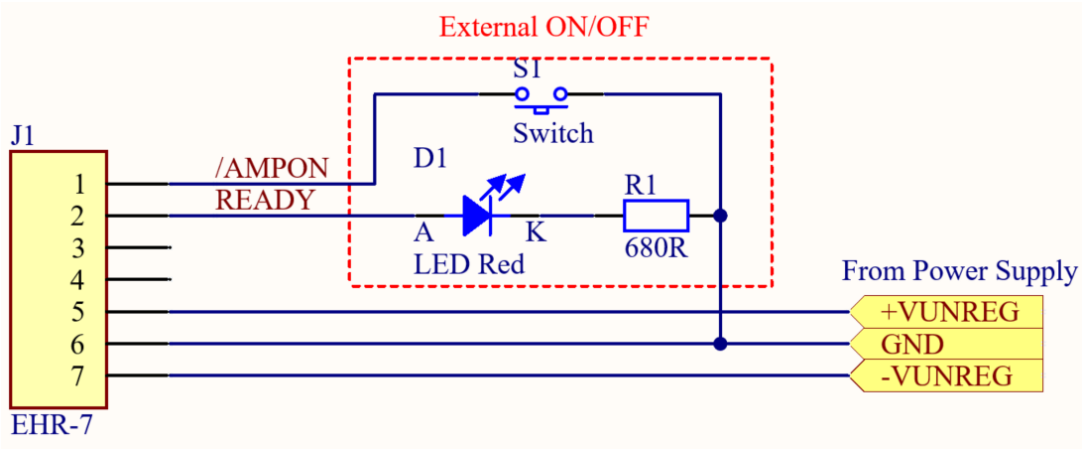


Figure 7 External ON/OFF Switch

8 Revision History

Rev	Date	Description	ID
(1.0)	2024-12	Initial version	KNM

Table 12 Revision History

1 EVM Use Restrictions and Warnings:

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