PURIFI

PURE SOUND

Building a Straight Wire to the Soul of Music

EVAL5
USER'S GUIDE

1 Introduction

This document describes the operation, function, and usage of the EVAL5 evaluation kit ("EVM") consisting of one 1ET9040BA amplifier module, one FE05 front-end module and a cable kit.

The EVM is provided for engineering evaluation and laboratory test purposes only. Great care should be taken when handling the EVM, especially when connected to power supplies and loads. Observe the voltage and power ratings and apply suitable precautions to protect the operator from electrical hazards.

Also note that the EVM is provided as an unshielded PCB assembly and should be protected from ESD as well as mechanical stress.

1.1 Setup and operation

1. Connect the 1ET9040BA module with the Front-End Board (FE05) using the ribbon cable supplied.
2. Place EVM on a flat surface; note that the amplifier base plate is connected to GND and should be attached to an external heatsink, e.g., a larger aluminum plate, for extended high power testing.
3. Connect external laboratory supplies (or other suitable PSU's) to FE05 and 1ET9040BA (refer to section 5)
4. Connect audio input and speaker (or other suitable load/test equipment)
5. Enable operation by pulling nENABLE signal to GND, by shorting J7 pin1-2 or J5 pin 6-1 on FE04
   A green LED will light up when all supply voltages are within operational range.
6. It is recommended to disable operation (set nENABLE signal high) and turn off all power supplies when module is not in use.

1.2 Power Testing

The amplifier module is protected from overheat via a thermal protection system that monitors the temperature of the aluminium base plate and the output inductors. The aluminium plate provides limited cooling, likely adequate for full-power music as well as for typical test sweeps etc., However, for continuous high power delivery additional cooling is required.

2 EVAL5 Overview

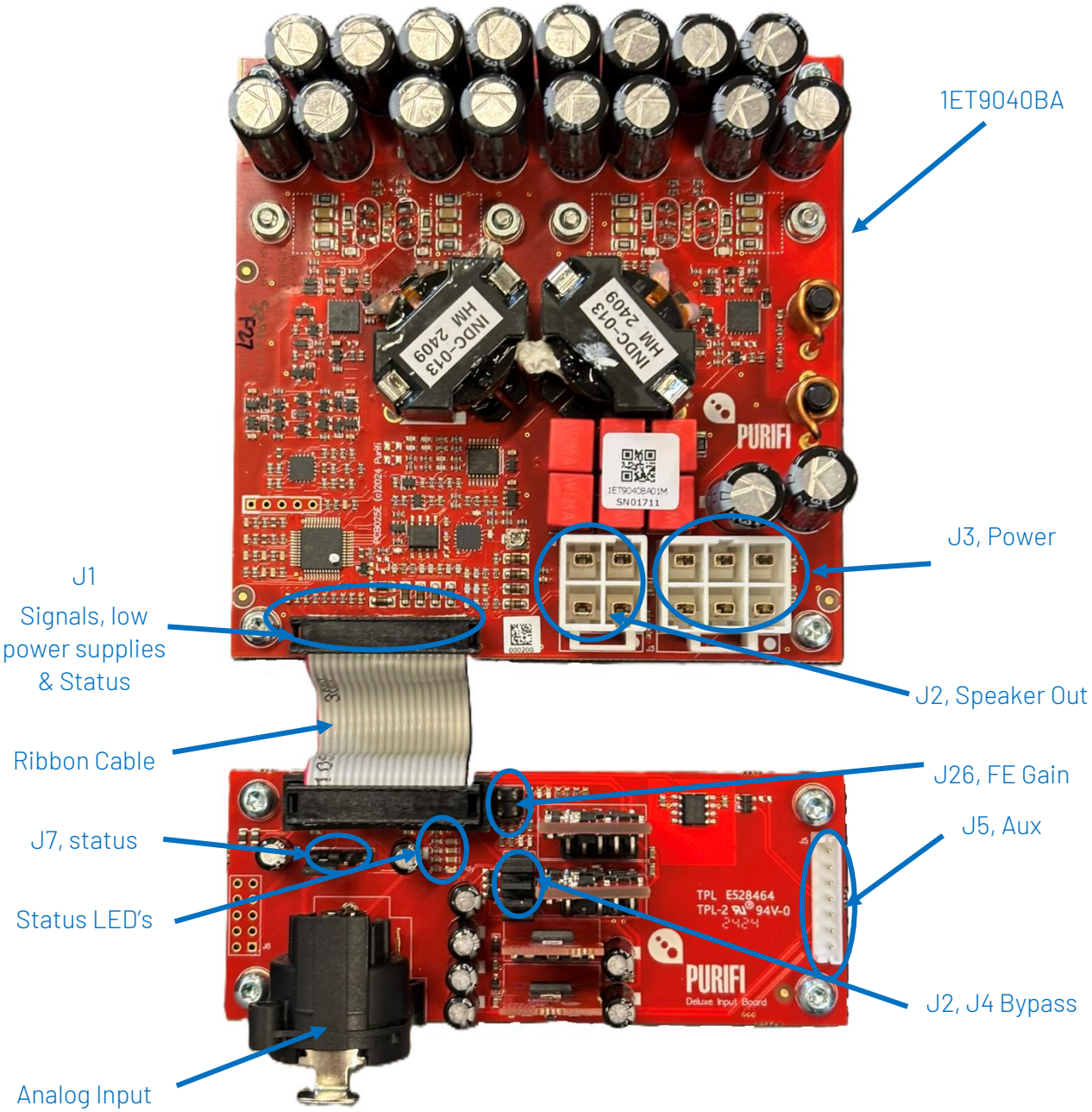


Figure 1 EVAL5 Overview

3 Interface, 1ET9040BA Amplifier Module

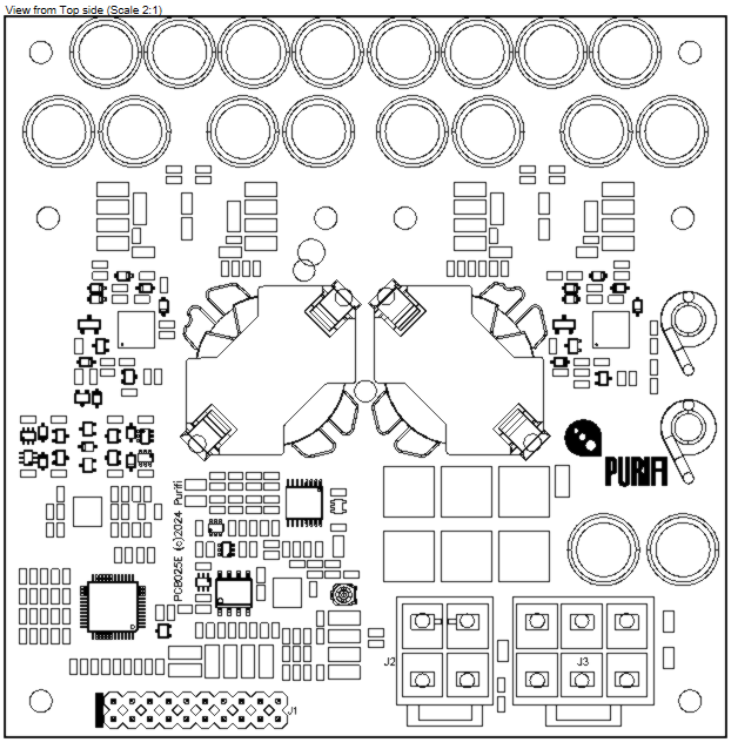
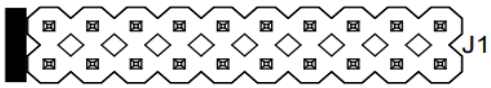


Figure 2 1ET9040 Amplifier Module

3.1 Main Connector, J1

Pin 2
Pin 1



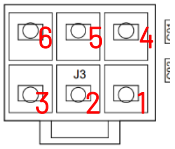
Pin 20
Pin 19

Pin	Signal	Rating	I/O	Description
1	GND		-	Common ground for all circuits
2	+5D		P	External Voltage supply logic-level circuits
3	READY		O	Amplifier "Ready" – "all good for operation" when high
4	/ENABLE		I	Amplifier Enable (HW Mode) – *pull low to enable Amp*
5	ICL		O	Output Current clipping
6	VCL		O	Output Voltage clipping
7	ADDR		I	Mode/I2C Address Selection; set by one 1% resistor
8	GPIO/INT		I/O	GPIO. Can be set up for error interrupt or logic input (SW mode)
9	SDA		I/O	I2C Data (SW Mode)
10	SCL		I/O	I2C clock (SW Mode)
11	/FATAL		O	Amplifier "error/fail" – signal goes low on error
12	+5A		P	External Voltage supply analog low-voltage circuits
13	GND		-	Common ground for all circuits
14	GND		-	Common ground for all circuits
15	IN+		I	Analog Input, positive
16	IN-		I	Analog Input, negative
17	GND		-	Common ground for all circuits
18	GND		-	Common ground for all circuits
19	+Vop		P	OPAMPs, positive rail
20	-Vop		P	OPAMPs, negative rail

Table 1 Main Connector, J1

Connector type equivalent: Molex 70246-2004
Mating cable part: Standard 20pole, 2-row 2.54mm pitch female connector.

3.2 Power connector, J3

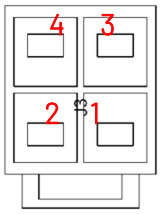


Pin	Signal	Rating	I/O	Description
1	VDR		P	Gate Drive Supply, referenced to -VP
2	+VP		P	Power Stage Supply, positive rail
3,6	GND		P	Ground
4,5	-VP		P	Power Stage Supply, negative rail

Table 2 Power connector, J3

Connector type equivalent: JST: B06P-VL
Mating cable part: JST: VLP-06V

3.3 Speaker Output Connector, J2



Pin	Signal	Rating	I/O	Description
1, 3	OUTH		P	Speaker Output, positive
2, 4	OUTC		P	Speaker Output, negative

Table 3 Speaker Output Connector, J2

Connector type: JST B04P-VL
Mating cable part: JST VLP-04V

4 Interface, FE05 Input Module

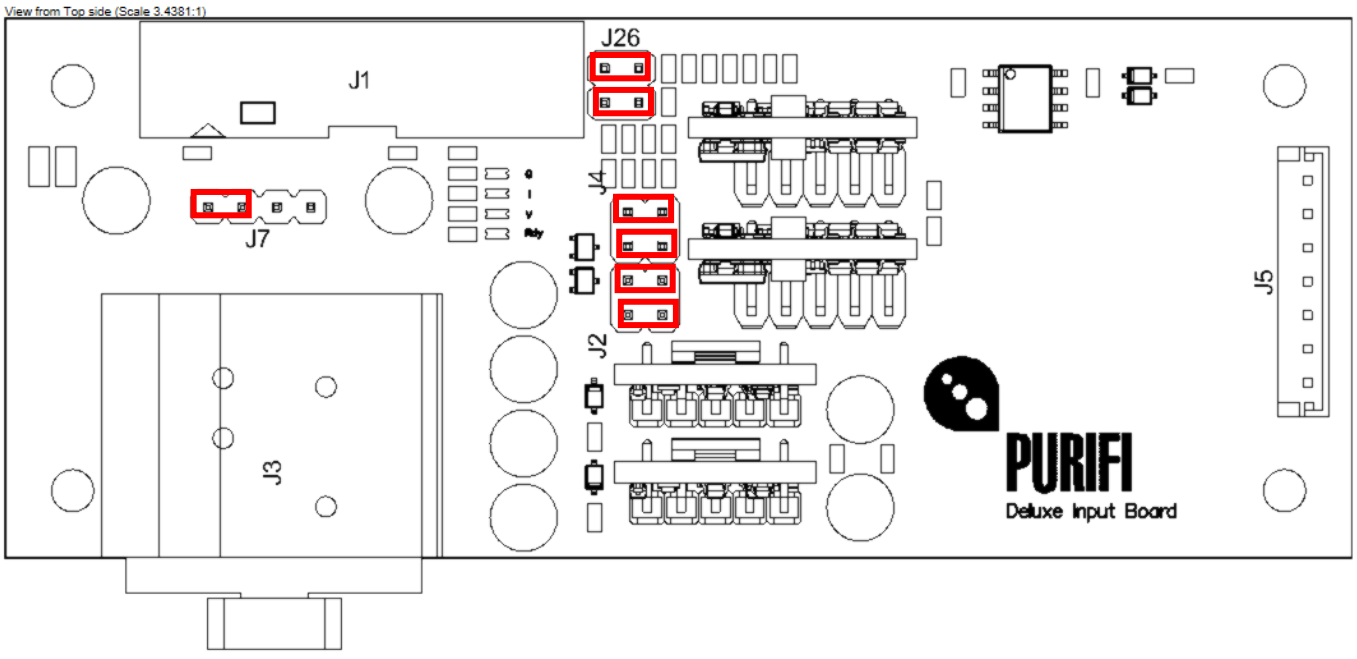


Figure 3 FE05 Input Module – with default Jumpers marked in red

4.1 Main Connector, J1

Same pinning as J1 on 1ET9040BA

Pin	Signal	Rating	I/O	Description
1	GND		-	Common ground for all circuits
2	+5D		P	External Voltage supply logic-level circuits
3	READY		O	Amplifier "Ready" – "all good for operation" when high
4	/ENABLE		I	Amplifier Enable (HW Mode) – *pull low to enable Amp*
5	ICL		O	Output Current clipping
6	VCL		O	Output Voltage clipping
7	ADDR		I	Mode/I2C Address Selection; set by one 1% resistor
8	GPIO/INT		I/O	GPIO. Can be set up for error interrupt or logic input (SW mode)
9	SDA		I/O	I2C Data (SW Mode)
10	SCL		I/O	I2C clock (SW Mode)
11	/FATAL		O	Amplifier "error/fail" – signal goes low on error
12	+5A		P	External Voltage supply analog low-voltage circuits
13	GND		-	Common ground for all circuits
14	GND		-	Common ground for all circuits
15	IN+		I	Analog Input, positive
16	IN-		I	Analog Input, negative
17	GND		-	Common ground for all circuits
18	GND		-	Common ground for all circuits
19	+Vop		P	OPAMPs, positive rail
20	-Vop		P	OPAMPs, negative rail

Table 4 Main Connector, J1

Connector type equivalent: Molex 70246-2004
Mating cable part: Standard 20pole, 2-row 2.54mm pitch female connector.

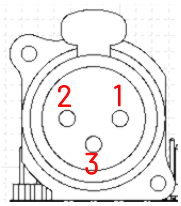
4.2 Aux connector 1, J5

Pin	Signal	Rating	I/O	Description
1	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
2	READY		O	Amplifier Ready – "all good for operation" when high
3	/FATAL		O	Amplifier "error/fail" – *signal goes low on error*
4	Vstb		P	Standby input to board 5V regulator, requires R147 mounted. For use when 1ET9040BA Microcontroller should be powered
5	+VUNREG		P	Voltage regulator input, positive rail
6	GND		P	Ground
7	-VUNREG		P	Voltage regulator input, negative rail

Table 5 Aux connector, J5

Connector type: JST: B7B-EH-A(LF)(SN)
Matching cable part: JST: EHR-7

4.3 Analog input XLR connector, J3

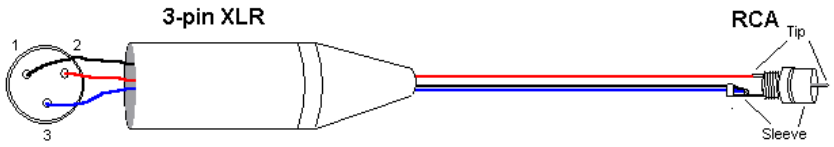


Pin	Signal	Rating	I/O	Description
1	GND		-	Ground
2	IN+		I	Analog input, positive
3	IN-		I	Analog input, negative

Table 6 Analog input XLR connector, J3

Connector type: Neutrik NC3FAH2
Mating Cable part: Standard 3-pin XLR male connector.

If a single ended input is need then connect GND and IN- to the negative analog input. When using the FE04 gain stage the single ended input is converted to a fully balanced signal and then fed to the 1ET9040BA module. The connection of the GND and IN- is best done at the source end.



4.4 Gain/Bypass jumpers, J26, J2 & J4

FE05 includes a pre-gain stage with selectable ~5.6dB to ~13.3dB gain. The pre-gain stage can be bypassed by location of two sets of jumpers (2.54mm pitch), enabling a total gain for EVAL5 between ~14.4dB (preamp bypass) to ~27.7dB to be selected:

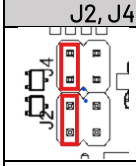
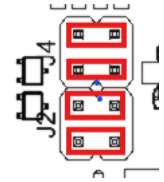
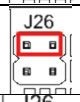
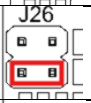
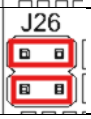
J2, J4	Jxx Description	J26	J26 Description	EVAL5 total gain	Input Impedance
	Pre-gain bypassed	-	-	14.4dB	1.5k ohm
	Pre-gain Enabled		~5.6dB pre-gain	~20.0dB	94k ohm
			~8.8dB pre-gain	~23.2dB	94k ohm
			~11.6dB pre-gain	~26.0dB	94k ohm
			~13.3dB pre-gain	~27.7dB	94k ohm

Table 7 Gain/Bypass jumpers, J26, J2 & J4

The pre-gain stage is made with two discrete OPAMPs configured as Balanced/single-ended to balanced gain stage as shown below:

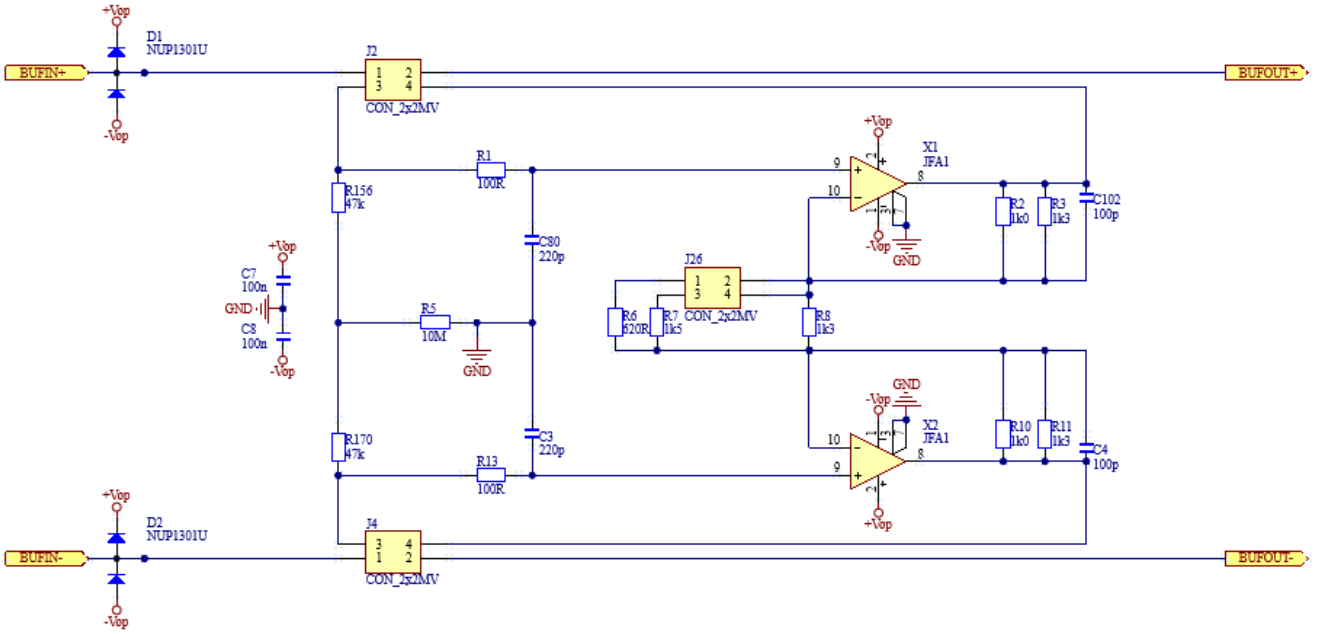


Figure 4 Preamp Schematic.

The gain stage can be enabled/by-passed with the help of pin headed J2/4 and jumpers as shown in Table 7.

4.5 Enable switch, J7

Pin	Signal	Rating	I/O	Description
1	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
2	GND		P	Ground
3	/FATAL		-	Amplifier "error/fail" – signal goes low on error
4	READY		O	Amplifier Ready – "all good for operation" when high

Table 8 Gain/Bypass jumpers, J15, J16 & J26

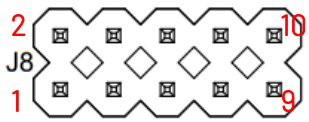
Connector type equivalent: Sullins PREC004SAAN-RC
Mating cable part: Standard 4pole, 1-row 2.54mm pitch female connector
An external switch to enable/disable amplifier operation, and status LED can be connected to J7.
For testing the EVAL5, a jumper can be mounted to connect pin 1 and pin 2 (default)

4.6 Status LED's

	LED	Signal	Description
R175 D29 G R146 D17 I R150 D18 V R151 D28 Rdy	Red	GPIO/INT	Interrupt signal
	Red	ICL	Current Clip Signal
	Red	VCL	Voltage Clip Signal
	Green	READY	Amplifier Ready – "all good for operation"

Table 9 Status LED's

4.7 I2C Connector, J8



Pin	Signal	Rating	I/O	Description
1	SCL		I/O	I2C Clock
2, 10	GND		P	GND
3	SDA		I/O	I2C Data
4-9	NC		-	Not connected

Table 10 I2C Connector, J8

Not mounted pr default, 10pin 2.54mm double row footprint.

5 Power Supplies

Refer to the figure below showing required power supplies and how to connect these to FE05:

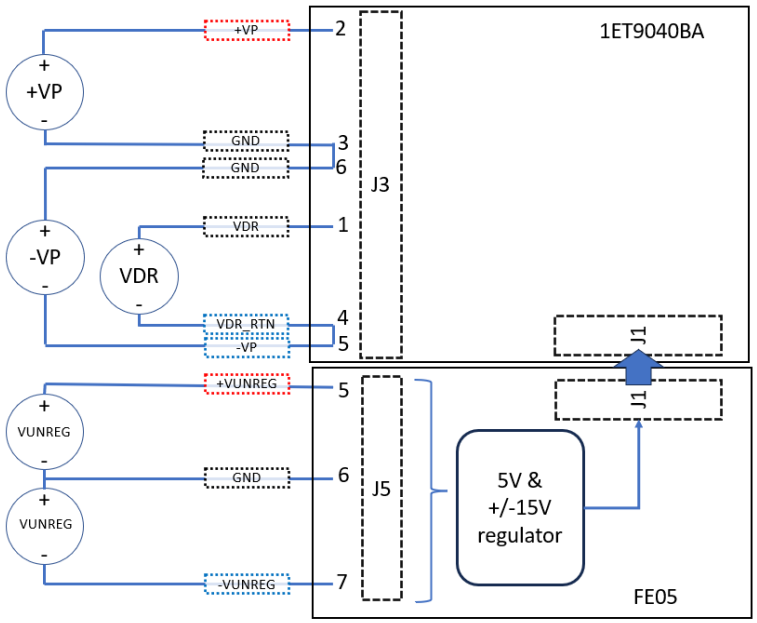


Figure 5 Power Supplies

All supply levels should be cross-checked with the Recommended Operation Conditions as specified in the respective amplifier module data sheet.

Recommended supply voltages for EVAL5 (please also refer to the 1ET9040BA Data Sheet):

Parameter		Min	Typ	Max	Unit
Power Supplies					
+VP	Power Stage, positive rail voltage	30	45	50	V
-VP	Power Stage, negative rail voltage	-50	-45	-30	V
VDR	Gate Drive, voltage (must be referenced to -VP)	14.25	15	15.75	V
+VUNREG	OPAMPs, positive rail voltage	16.5	18	25	V
-VUNREG	OPAMPs, negative rail voltage	-25	-18	-16.5	V

Table 11 Recommended Supply Voltages

5.1 Linear Regulators

FE05 includes two discrete voltage regulators for the OPAMP's negative and positive supply voltages (+VOP and -VOP) and a 5V regulator for the logic and analog low voltage circuits (+5D & +5A).

6 Operating Modes & Status Reporting

6.1 Mode Configuration

The EVAL5 can be used with either HW or SW control:

1. HW Mode: all control and status via pins (HW interface)
2. SW Mode: enables control and status via I2C interface
   The address selector resistor, R145, is populated with 27kohm setting the address to 0x58. See datasheet for the other address options.

6.2 HW Mode

The amplifier module is controlled via the /AMPON control signal. /AMPON is available on connectors J5 and J7 and can be controlled via external source.

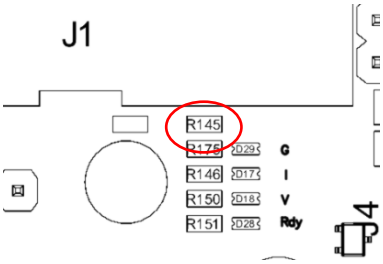
Amplifier status is signaled via READY, ICL, VCL, GPIO/INT and /FATAL:

READY signal is connected to a green LED on FE05, and is pinned out on connector J5 & J7
ICL, VCL and GPI/INT are connected to RED LEDs on FE05
/FATAL signal is connected to a RED LED and pinned out on connectors J5 & J7.

6.3 SW Mode

SW Mode enables controlled on/off and reading status registers via I2C.
Setup of the GPIO pin function is also available in SW mode
The I2C register map can be found in the amplifier data sheet.

I2C is accessed via SCL, SDA on connector J8, this connector is per default not mounted.



The I2C address can be programmed via the value of resistor R145 on FE05. Refer to the **Mode Selection ADDR** table in the amplifier data sheet for information on resistor value vs. I2C address.

7 Mechanical Specifications & System Considerations

7.1 EVAL5 Dimensions

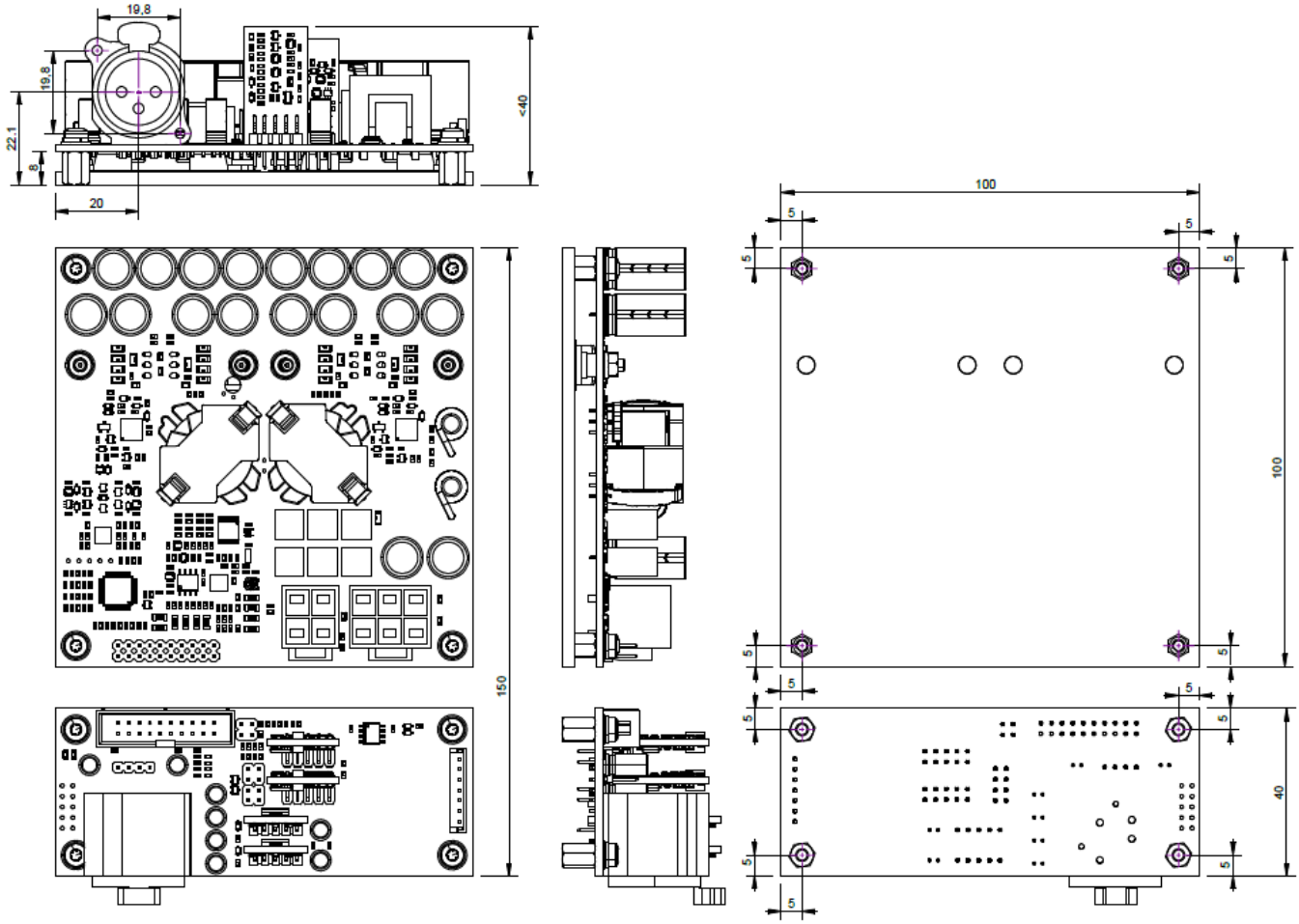


Figure 6 1ET9040BA Dimensions.

7.2 Thermal Requirements

While 1ET9040BA has very low idle losses and high overall efficiency, adequate cooling is essential for sustained power delivery. Careful consideration must be given to designing the thermal system to achieve desired output power specifications.

It is recommended to mount the module on a heatsink, e.g., an adequately designed aluminum chassis.

7.3 Mechanical Requirements

Related to mechanical robustness of the end application, it is the reasonability of the system integrator to specify process, materials, locations, etc. for e.g., gluing of critical components which may be required and to prove/document short- and long-term performance and reliability. The system integrator must ensure integrity of mounting methods and materials used related to fixation of the module. It is recommended to thoroughly test the final product for robustness against, e.g., shock and vibration.

7.4 Compliance Testing

1ET9040BA is designed with considerations for compliance of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required.

8 Revision History

Rev	Date	Description	ID
(1.00)	2025-03	Initial Revision	KNM

Table 12 Revision History

1 EVM Use Restrictions and Warnings:

1.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS. 1.2 User must read and apply the user guide and other available documentation provided by PURIFI ApS regarding the EVM prior to handling or using the EVM. 1.3 Safety-Related Warnings and Restrictions: 1.3.1 User shall operate the EVM within PURIFI ApS's recommended specifications and environmental considerations stated in the specification or other available documentation provided by PURIFI APS, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM documentation prior to connecting any load to the EVM output. During normal operation, even with the inputs and outputs are kept within the specified allowable ranges, some circuit components may have elevated case temperatures. When working with the EVM, please be aware that the EVM may become very warm. If there is uncertainty as to the ratings and specifications, please contact PURIFI ApS prior to connecting interface electronics including input power and intended loads. 1.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees. 1.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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