PURIFI

PURE SOUND

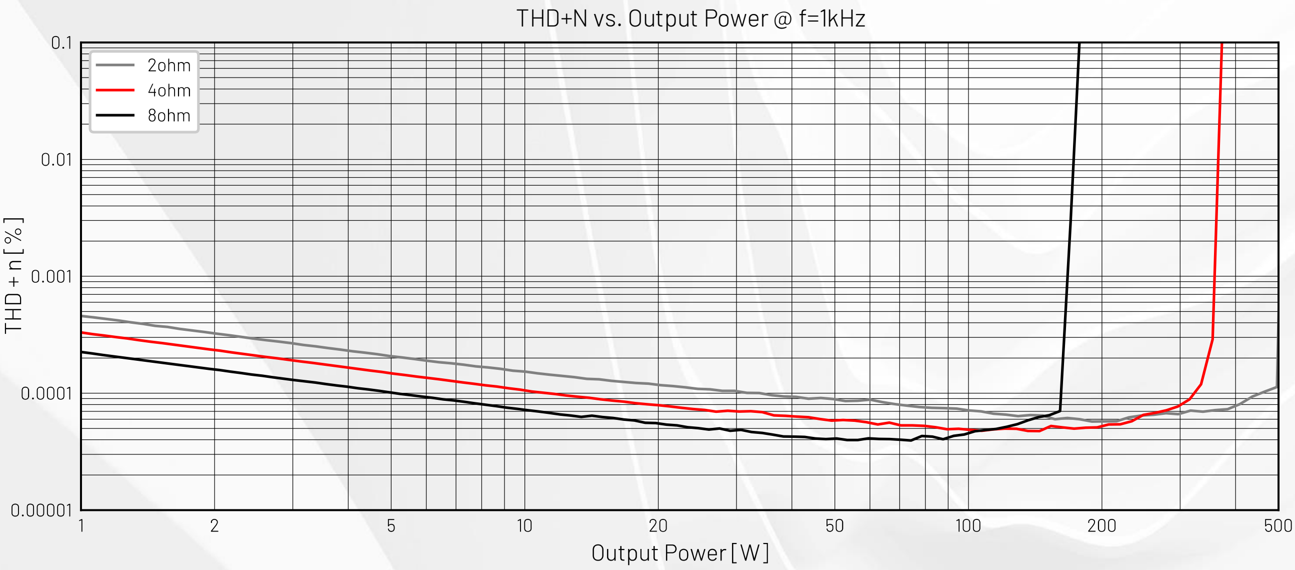
Building a Straight Wire to the Soul of Music

1ET6525SA DATA SHEET

KEY SPECIFICATIONS

- 2nd Generation EIGENTAKT
- Single-channel, analog-input Class D amplifier module
- Negligible THD and IMD
- Extraordinarily Low Noise
- Load-invariant Response
- Exceptionally Clean Clipping
- Low Losses & High Efficiency

Output Power	>450W @ 1% THD, 4Ω
Output Current	~25A
THD+N	<0.0001% (-120dB) @ 100W, 4Ω, 20-20kHz
Dynamic Range	~137dB(A)
Output Noise	~6.6μV(A)
Gain	12.3dB
Output Impedance	<30μΩ @ 1kHz
Efficiency	>94%
Idle losses (output stage)	~1.6W
Supply	±32V to ±65V DC
Size	82x63x33mm



1 Specifications

1.1 Absolute Maximum Ratings

Referenced to GND unless otherwise noted.

	Parameter		Min	Max	Unit
Power Supplies	Power Stage Supply, positive rail voltage (+VP)		-0.3	75	V
	Power Stage Supply, negative rail voltage (-VP)		-75	0.3	V
	Gate Drive Supply, voltage, referenced to -VP (VDR)		-0.3	20	V
	OPAMPs supply, positive rail voltage (+VOP)		-0.3	20	V
	OPAMPs supply, negative rail voltage (-VOP)		-20	0.3	V
	Digital Supply, voltage (VD) (optional use)		-0.3	20	V
I/O's	Analog Inputs (+AIN, -AIN)		-15	15	V
	Logic-level outputs, continuous current (SMPS_OFF, READY)			50	mA
	Logic-level inputs, voltage (/AMPON, SDA, SCL, /FATAL)		-0.3	5.3	V
		+VOP < 5.5V, 0V < VD < 5.5V	-0.3	VD	V
	Open-drain, bi-directional, continuous current (SDA)			50	mA
Env.	Ambient temperature		0	100	°C
	Heatsink temperature		0	100	°C
	Relative Humidity, non-condensing			85	%

Stress beyond Absolute Maximum Ratings may cause permanent damage to the Design and associated circuitry. Attempts to operate the Design within Absolute Maximum Rating but outside Recommended Operation Conditions (Table 2) may result in non-functional circuits and erroneous behavior.

Table 1 Absolute Maximum Ratings

1.2 Recommended Operating Conditions

Amplifier operation is permitted only under conditions stated in Table 2.

Referenced to GND unless otherwise noted.

	Parameter	Min	Typ[1]	Max	Unit
Power Supplies					
+VP	Power Stage, positive rail voltage	32	65	70	V
-VP	Power Stage, negative rail voltage	-70	-65	-32	V
VDR	Gate Drive, voltage (must be referenced to -VP)	13.6	15	16.5	V
+VOP	OPAMPs, positive rail voltage	11.4	12	16.5	V
-VOP	OPAMPs, negative rail voltage	-16.5	-12	-11.4	V
VD	Digital, voltage (optional use)	4	5	16.5	V
I/O's					
V_{in_dif}	Analog Inputs, differential rms voltage (pos. to neg. input)[2]	-15.5		15.5	V
V_{in_cm}	Analog Inputs, common-mode voltage	-5	0	5	V
R_L	Speaker Load, resistive	2[3]	4	∞	Ω
Z_L	Speaker Load, capacitive		0	1	µF
Environmental					
T_A	Ambient temperature	0	25	60	°C
T_{HS}	Heatsink temperature	0	25	75	°C
θ_{HS-A}	Thermal resistance, Heatsink to Ambient		see note[4]		°C/W
RH	Humidity, relative (non-condensing)		50	85	%

1) Audio Performance Specs are not guaranteed outside Typ. recommended operating conditions.
2) +/-15Vpeak corresponds to approximately full rated power (1% THD) in typ. load condition
3) The amplifier is stable into loads <2Ω. Output power into impedances <3.2 Ω may be limited by the Over Current Protection system.
4) The required θ_{HS-A} depends highly on the desired sustained power delivery specification – see section 7.2)

Table 2 Recommended Operating Conditions

1.3 Audio Characteristics

R_L=4Ω, T_A=25° free operating air, f=1kHz, 20kHz AES17 filter (AP), typical operating conditions (Table 2) unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
P_O	Output Power, Short term	R_L= 8Ω, 1%THD		230		W
		R_L= 4Ω, 1%THD		450		W
		R_L= 2Ω, 1%THD		510[1]		W
	Output Power, Continuous[2]	-		(as limited by thermal system)		-
THD+N	Total Harmonic Distortion + Noise	P_O=1W, f=1kHz		0.00035		%
		P_O=10W, f=1kHz		0.0001		%
		P_O=100W, f=1kHz		0.00005[3]		%
		P_O=1W, f=20-20kHz		0.00035		%
		P_O=10W, f=20-20kHz		0.00029		%
		P_O=100W, f=20-20kHz		0.0001[3]		%
IMD	Intermodulation Distortion, CCIF	P_O=1W, f=18.5kHz+19.5kHz		0.0000003		%
		P_O=10W, f=18.5kHz+19.5kHz		0.0000006		%
		P_O=100W, f=18.5kHz+19.5kHz		0.0000005		%
	Dynamic Intermodulation Distortion, DIM	P_O=1W, DIM30		0.002[3]		%
		P_O=10W, DIM30		0.002[3]		%
		P_O=100W, DIM30		0.009[3]		%
ICN	Idle Noise, speaker output	A-weighted		6.6		µV
DNR	Dynamic Range	A-weighted, relative 450W, R_L= 4Ω		137		dB
SNR	Signal to Noise Ratio	A-weighted, relative to 450W, R_L= 4Ω		137		dB
BW	Frequency Response, upper -3dB/-6dB	R_L= 8Ω, V_o=2.83V@1kHz (=1W)		80/100		kHz
		R_L=4Ω, V_o=2.83V@1kHz		80/100		kHz
		R_L= 2Ω, V_o=2.83V@1kHz		80/100		kHz
	Frequency Response, lower -3dB	-		(DC coupled)		-
	Frequency Response, flatness	R_L= 8Ω, f= 20-20kHz		±0.01		dB
		R_L= 4Ω, f= 20-20kHz		±0.01		dB
		R_L= 2Ω, f= 20-20kHz		±0.01		dB
		R_L= ∞Ω, f= 20-20kHz		±0.01		dB
	Frequency Response, load variation	R_L= 2 -∞Ω, f= 20-20kHz		±0.01		dB
Z_O	Output Impedance[4]	1kHz, I_{out}=1A		0.03		mΩ
		20-20kHz, I_{out}=1A		<0.35		mΩ

1) Power is limited by overcurrent protection system (OCP)
2) Continuous output power depends on properties of the thermal system. With adequate thermal interface from the aluminum back plate to case / heatsink all power ratings are continuous power provided the aluminum backplate temperature is within recommended operating conditions. Data provided is based on module operating in free air.
3) THD @ 100W and DIM readings limited by analyzer
4) Kelvin (4-terminal) measurement on edge connector.

Table 3 Audio Characteristics

1.4 Typical Audio Performance, Graphs

T_A=25° free operating air, 20kHz AES17 filter (AP), typical operating conditions (Table 2) unless otherwise noted.

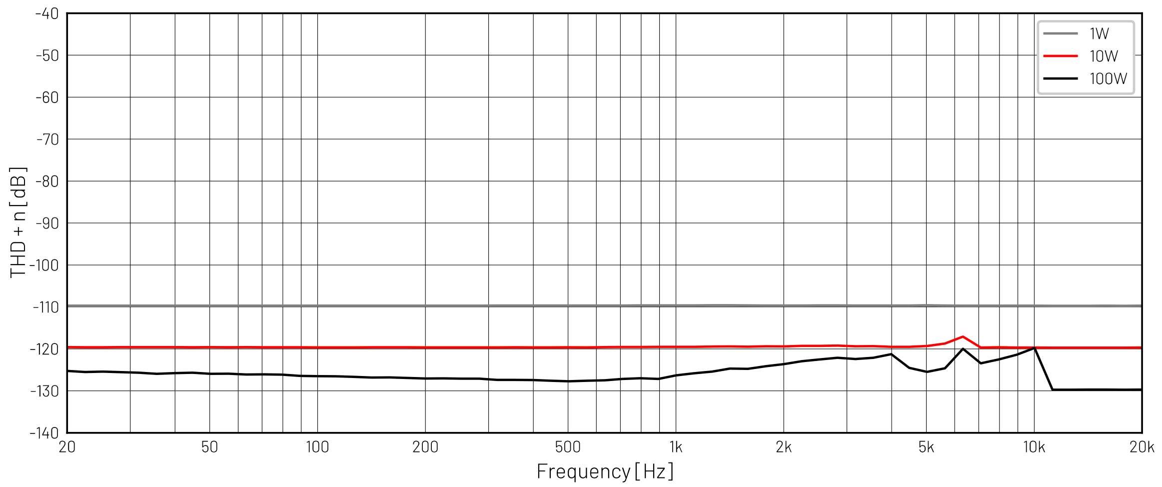


Figure 1 THD [dB] vs. Frequency @ 4Ω

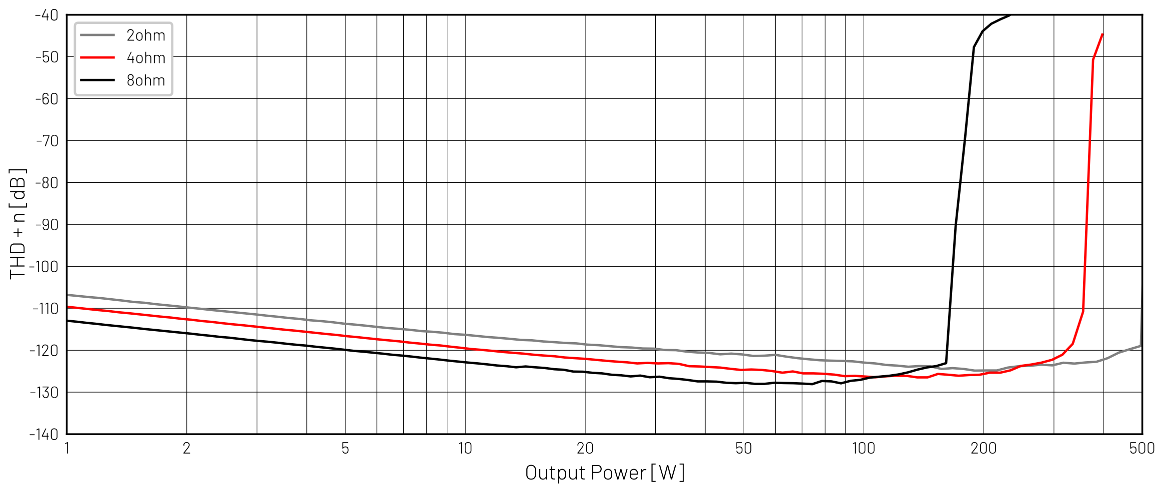


Figure 2 THD+N [dB] vs. Power @ f=1kHz

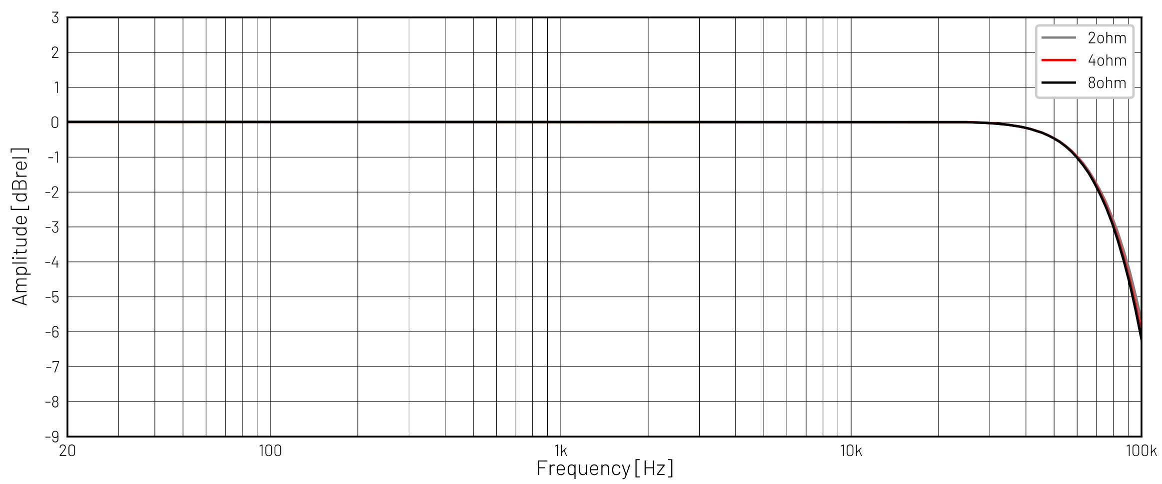


Figure 3 Frequency Response @ V_i=2.83V

T_A=25° free operating air, 20kHz AES17 filter (AP), 16K/48kHz/32x avg. FFT's, Equiripple window, typical operating conditions (Table 2) unless otherwise noted.

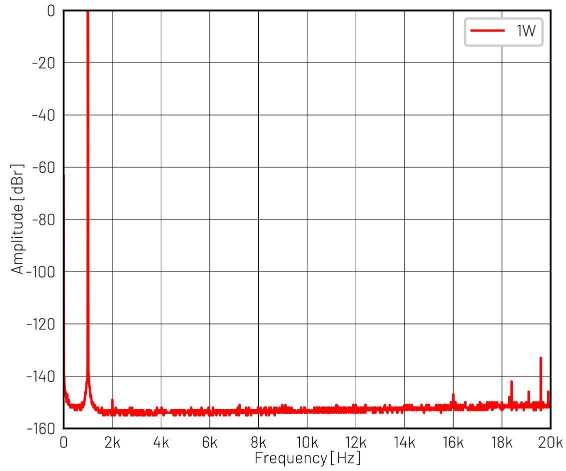


Figure 4 Frequency Spectrum (FFT) @ 1kHz, 1W, 4Ω

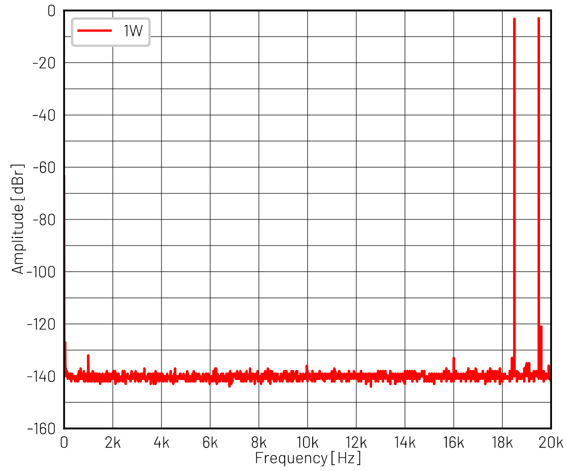


Figure 5 Intermodulation Distortion @ 18.5+19.5kHz, 1W, 4Ω

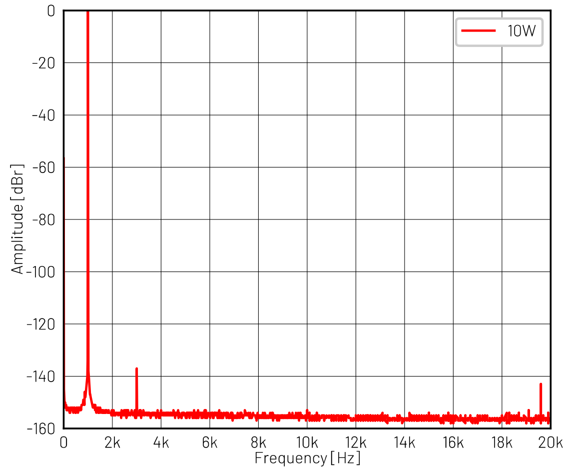


Figure 6 Frequency Spectrum (FFT) @ 1kHz, 10W, 4Ω

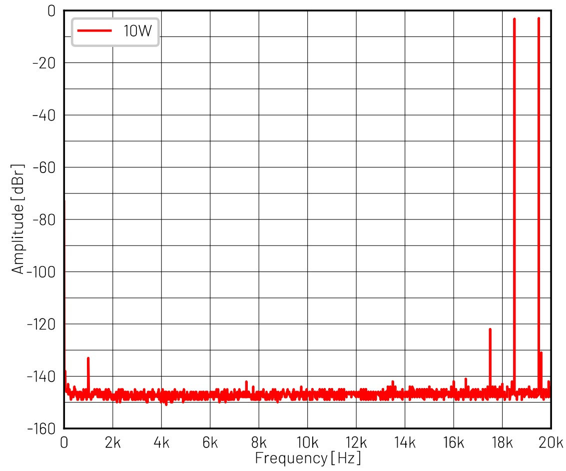


Figure 7 Intermodulation Distortion @ 18.5+19.5kHz, 10W, 4Ω

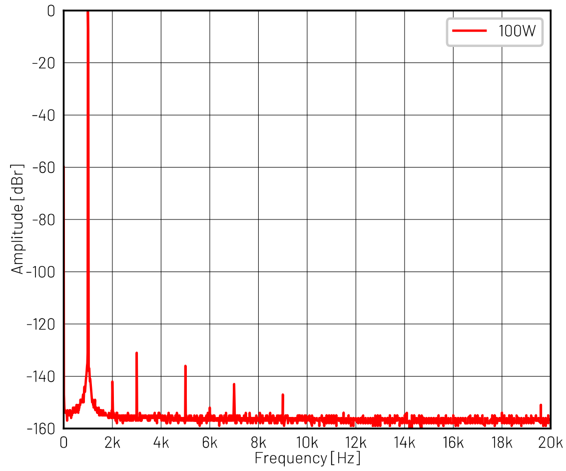


Figure 8 Frequency Spectrum (FFT) @ 1kHz, 100W, 4Ω

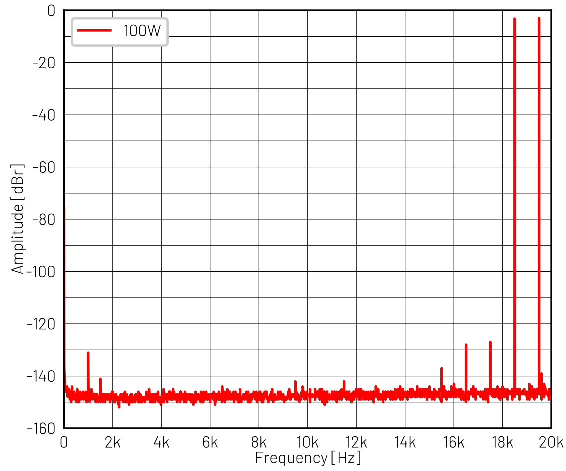


Figure 9 Intermodulation Distortion @ 18.5+19.5kHz, 100W, 4Ω

T_A=25° free operating air, 20kHz AES17 filter (AP), typical operating conditions (Table 2) unless otherwise noted.

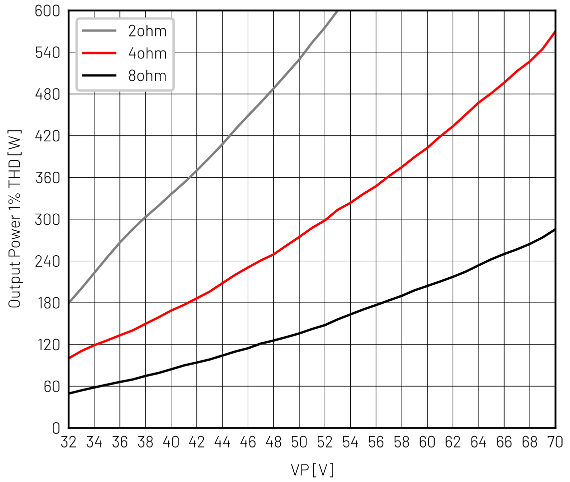


Figure 10 Output Power vs. VP @ 1% THD

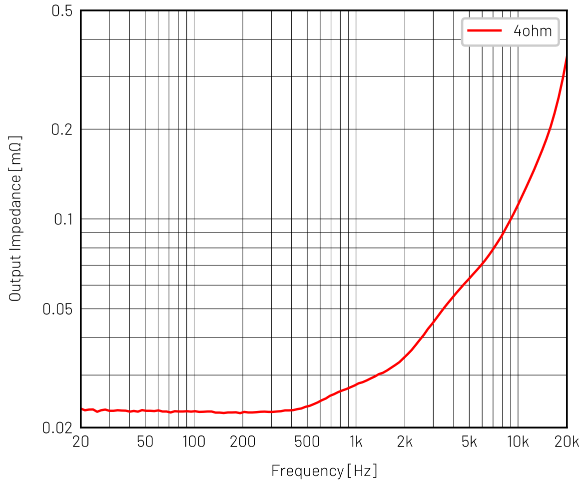


Figure 11 Output Impedance vs. Frequency

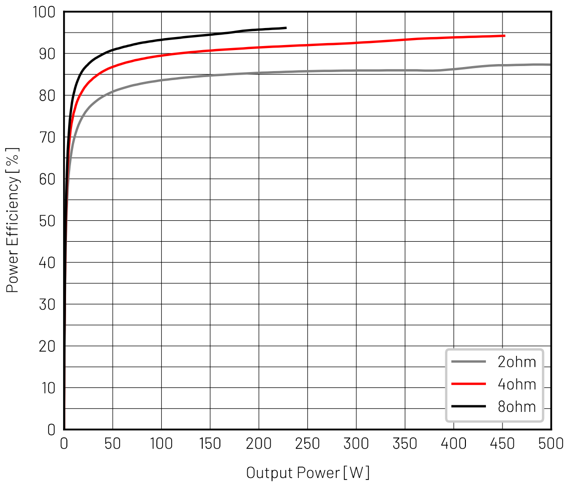


Figure 12 Power Stage Efficiency vs. Output Power

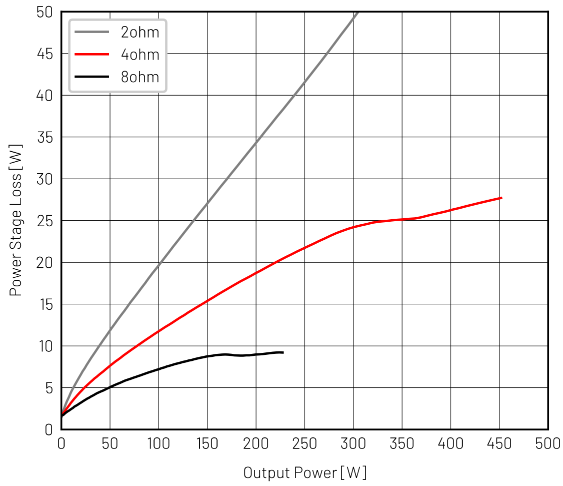


Figure 13 Power Stage Loss vs. Output Power (one channel)

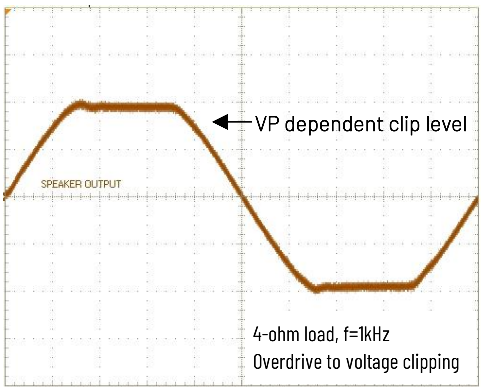


Figure 14 Voltage Clipping/Recovery (behavior)

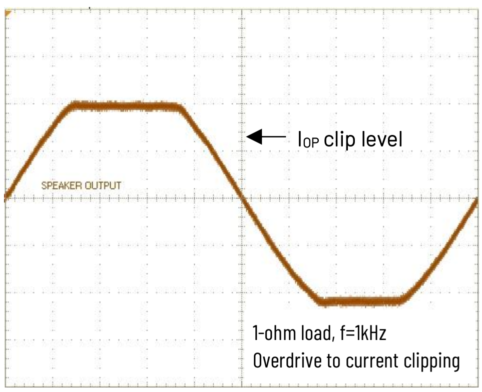


Figure 15 Current Clipping/Recovery (behavior)

1.5 Electrical Characteristics

Typical operating conditions (Table 2), f=1kHz, unless otherwise noted.

Parameter		Conditions	Min	Typ[1]	Max	Unit
Current Consumption & Efficiency						
$\lvert I_{VP} \rvert$	Power Stage supply, current	(+VP,-VP), Idle		12		mA
I_{DR}	Gate Drive supply, current	(VDR), Normal operation		50		mA
$\lvert I_{OP} \rvert$	OPAMPs supply, current	(+VOP, -VOP), Normal operation		25		mA
I_{VD}	uC and logic supply, current	(VD), Normal operation		7.5		mA
		(VD), Amplifier not switching		2.5		mA
η	Efficiency	R_L= 8Ω		96		%
		R_L= 4Ω, Full rated power		94		%
Audio Inputs & Output						
R_{in}	Input impedance	Differential, pos. to neg. input		2.2		kΩ
		Single-ended, input to GND, positive input (IN+)		5.2		kΩ
		Single-ended, input to GND, negative input (IN-)		1.1		kΩ
A_V	Voltage Gain	V_o/V_i		12.3		dB
$V_{in\_1\%THD}$	Differential input voltage	To get 1%THD @ R_L= 4Ω, VP=±65V [1]		10.8		V_{rms}
CMRR	Common Mode Rejection Ratio	Audio input, 1kHz		>60		dB
PSRR	Power Supply Rejection Ratio	Forced 1Vrms f≤1kHz ripple, either rail		>90		dB
$\lvert V_{o\_DC} \rvert$	Speaker Output, DC offset	Grounded analog inputs		<10		mV
f_s	Switching frequency	Idle (indicative)		550		kHz
		Positive clipping		>50		kHz
		Negative clipping		0		Hz
Logic Control Signals						
V_{IH}	High level input threshold	(/AMPON)	2.7			V
V_{IL}	Low level input threshold	(/AMPON)			0.65	V
V_{IH_I2C}	High level input threshold	(SDA)	2.3			V
V_{IL_I2C}	Low level input threshold	(SDA)			1	V
V_{OH_I2C}	High level output voltage	(SDA) Open-drain I=6mA	2.6			V
V_{OL_I2C}	Low level output voltage	(SDA) Open-drain I=10mA			0.6	V
I_{OL_I2C}	Low level sink current	(SDA) Open-drain			10	mA
V_{IH_SCL}	Open collector input	(SCL)	1.65			V
V_{IL_SCL}	Open collector input	(SCL)			0.5	V
I_{IH_SCL}	Open collector input	(SCL)			0.001	mA
I_{IL_SCL}	Open collector input	(SCL)			1	mA
I_{OOC}	Open collector output	(/FATAL)			10	mA
V_{OOC}	Open collector output	(/FATAL)			65	V
V_{OH}	High level output voltage	(READY, PSUDIS)	VD-0.7[2]	5		V
V_{OL}	Low level output voltage	(READY, PSUDIS)			0.6	V
Protection Systems						
I_{OCP}	Overcurrent Protection, threshold	Current limit		25		A
f_{DCP}	DC Protection, Speaker terminal	Detection filter corner frequency		2.5		Hz
$\lvert V_{DCP} \rvert$		Voltage limit, low-pass filtered signal		12		V
T_{OTP}	Thermal Protection, Heatsink	Over-temperature, 2°C hysteresis		75		°C
T_{UTP}		Under-temperature, 2°C hysteresis		0		°C
$\lvert OVP_{VP} \rvert$	Overvoltage Protection, threshold	(+VP, -VP), 1V hysteresis		75		V
OVP_{DR}		(VDR), 0.5V hysteresis		17.5		V
$\lvert OVP_{OP} \rvert$		(+VOP, -VOP), 0.5V hysteresis		18		V
$\lvert UVP_{VP} \rvert$	Undervoltage Protection, threshold	(+VP, -VP), 1V hysteresis		32		V
UVP_{DR}		(VDR), 0.5V hysteresis		13		V
$\lvert UVP_{OP} \rvert$		(+VOP, -VOP), 0.5V hysteresis		11		V

1) Performance depends on physical implementation and system-level circuitry/configuration. Data provided is based on module operating in free air.
2) If 5V > VD > +VOP, V_{OH} min will be VD-0.7V

Table 4 Electrical Characteristics

1.6 Timing Characteristics

Typical operating conditions unless otherwise noted.

Parameter		Conditions	Min	Typ[1]	Max	Unit
Control Signals						
/AMPON	Mute time	Pin asserted high to Amp output HiZ		1		ms
/AMPON	Un-mute time	Pin asserted low to Amp output LoZ		1.25		ms
READY	Start delay	Supplies stable to READY asserted high		1.25		ms
/FATAL	Amplifier failure to signal assertion	Failure to /FATAL low		40		ms
PSUDIS	PSU off signal	DC failure to PSUDIS high		40		ms
HS/ADDR	Mode Selection	Power-up to Mode latched		10		ms
Protection Systems						
t_{OCP}	OCP Mute cycle duration	OCP event to reenable outputs		>300		ns
OLP	Overload Protection, threshold	Ratio of OCP cycles to non-OCP cycles		12		%
t_{OLP}	OLP Mute cycle duration	OLP even to reenable outputs		1		s
t_{DCP}	DCP Mute cycle duration	DCP even to reenable outputs		1		s

1) Performance depends on physical implementation and system-level circuitry/configuration. Data provided is based on module operating in free air.

Table 5 Timing Characteristics

1.7 Mechanical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
SIZE	Length			82		mm
SIZE	Width			63		mm
SIZE	Height			33	36	mm
Mounting[1]	Threaded standoff, heatsink-PCB, M3	Height		6		mm
Mounting[1]	Threaded stud, heatsink-FET-PCB	Length		13		mm
Mounting[1]	Spacer, FET-PCB, M3	Height		3		mm
Mounting[1]	Threaded standoff	Diameter		M3		-
Mounting[1]	Threaded standoff	Available thread depth			4	mm
Mounting[1]	Threaded standoff	Torque			0.5	Nm

1) The aluminum back plate is connected to GND and can be mounted electrically in contact with chassis GND. Do not use the aluminum back plate/threaded mounting holes for power supply connection.

Table 6 Mechanical Characteristics

2 Introduction

The 1ET6525SA is a single-channel, ultra-high-performance, analog-input Class D amplifier module capable of delivering over 450W of power. It sets a new benchmark for audio quality across all amplifier classes. By leveraging 2nd generation Eigentakt ErrorCorrection, it achieves the highest level of performance. Its compact size and exceptional reliability make it suitable for a wide range of applications, while its superior sound quality makes it the clear choice for applications where audio excellence is paramount.

PURIFI's ongoing research in nonlinear control theory has led to the development of the first mathematically precise large-signal model for self-oscillating amplifier controllers. This breakthrough enables the complete optimization of the feedback circuit, resulting in performance improvements of at least an order of magnitude over existing designs. Additionally, the amplifier module features a comprehensive protection system, ensuring robustness and ease of integration.

These circuits and methods provide many practical and audible benefits:

- ***High loop gain (>85dB) in the entire audio band (2nd generation Eigentakt ErrorCorrection)***
  - *This figure corresponds to an unprecedented 356MHz Gain-Bandwidth Product and produces consistent ultra-high performance across the audio spectrum unmatched by audio amplifiers of any technology or operating class.*
- ***Negligible intermodulation distortion (IMD)***
  - *A very good measure for how well an amplifier handles complex signals. Sonically low IMD means a highly resolved and stable stereo image across the whole spectrum, even during very complex and busy passages.*
- ***THD remains extremely low at any frequency and any power level** right until clipping*
  - *Translates into a total lack of sonic signature, and an ability to reproduce any type of music without preference for genre or production style.*
- ***Negligible output noise***
  - *No audible noise. Deep black silence and a generous and detailed sound even at very low playback volumes.*
- ***High power supply rejection ratio (PSRR)***
  - *The module places no particular demands on the power supply quality. A simple off-the-shelf unregulated SMPS will not degrade audio performance.*
- ***Load-invariant frequency response and negligible output impedance***
  - *The amplifier handles difficult loudspeakers with ease, including those that challenge most other amplifiers.*
- ***Controlled, second-order low-pass response***
  - *Very flat audio-band response with a sensible, 80kHz bandwidth.*
  - *Reduced sensitivity to out-of-band noise from DACs, reducing the requirements on the DAC reconstruction filter. This leaves a shorter signal path between DAC and loudspeaker.*
  - *Problem-free operation with outboard DACs over which you may have no control.*
- ***Very low idle losses and reduced electromagnetic interference (EMI)***
  - *The enormous loop gain allows relaxed timing of the power MOSFETs without degrading audio performance.*
  - *Idle losses are minimized.*
  - *Very little to no effort needed to pass regulatory tests.*
- ***Exceptionally clean clipping and clipping-recovery** in both voltage and current domains*
  - *Clips cleanly and recovers immediately without "overhang". Current limiting is equally instantaneous and glitch free. This guarantees the smallest amount of audible artefacts when pushed into clipping or overload protection.*
- ***Overall implementation/integration ease** saves time and cost for the system integrator*
  - *Architecture completely eliminates heterodyning in multichannel applications.*

3 Overview

Figure 16 1ET6525SA top view

3.1 Edge Connector, J3

Pin	Signal	Rating	I/O	Description
Power Supplies				
1, 2	+VP		P	Power Stage Supply, positive rail
3,4,5 6,7,8	GND		-	Ground
9,10	-VP		P	Power Stage Supply, negative rail
11	VDR	Table 2	P	Gate Drive Supply, referenced to -VP
12	VD		P	(optional use) External Voltage supply to on-board 5V regulator
26	+VOP		P	OPAMPs, positive rail
25	-VOP		P	OPAMPs, negative rail
27	GND		-	Ground
I/O's				
13,14,15, 16,18	OUT-		O	Speaker Output, negative (internally connected to GND)
20,21,22, 23,24	OUT+		O	Speaker Output, positive
17, 19, 28,33,34	NC		-	Not connected
29	IN+		I	Analog Input, positive
30	IN-	Table 2	I	Analog Input, negative
31	HS/ADDR		I	Mode/I2C Address Selection; set by one 1% resistor.
32	PSUDIS /AMPON		O I	PSU off control signal (SW Mode), or Amplifier Disable (HW Mode) – *pull low to enable Amp*
35	SDA READY		I O	I2C Data (SW Mode), or Amplifier Ready (HW Mode) – "all good for operation" when high
36	SCL /FATAL		I O	I2C clock (SW Mode), or Amplifier "error/fail" (HW Mode) – *signal goes low on error*
Aluminum Backplate				
	GND		-	Ground. Do not use the aluminum backplate to connect power supply GND connections

Table 7 Edge Connector, J3

4 Power Supply, Control Signals & I/O's

4.1 Power Supply

Refer to below figure showing required power supplies and how to connect these to 1ET6525SA:

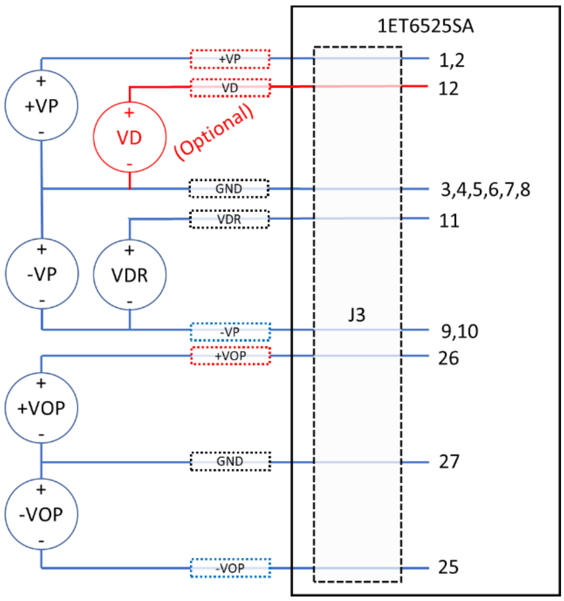


Figure 17 Power Supplies

Voltage, current and power ratings are described in detail in Table 2 Recommended Operating Conditions and Table 4 Electrical Characteristics.

4.1.1 Power Stage Supply (+VP, -VP)

1ET6525SA requires a ground-centered split-rail supply for the amplifier output stage.

Multiple factors need to be considered when determining capabilities of this supply, e.g., peak/continuous audio power requirements, nominal/minimum (speaker) load, thermal constraints and time constants/durations etc.

Refer to Figure 10 to determine required DC voltage based on desired nominal output power.

For a given supply voltage and output power specification, the power supply peak power and peak current can be estimated:

$$P_{psu\_peak} = 2\frac{P_{out\_rms}}{\eta} \quad ; \quad I_{psu\_peak} = \frac{P_{psu\_peak}}{VP}$$

The supply should be designed such that each rail has enough thermal headroom to drive full peak power for a minimum of one half-period of the lowest desired audio frequency or as otherwise required for continuous power delivery as determined by the system integrator. The 1ET6525SA design limits power delivery only if OCP or OTP events are triggered and in practice, especially in multichannel applications, the power supply often is the limiting factor for sustained power delivery.

Although 1ET6525SA includes over- and under-voltage protection (OVP/UVP) the power supply designer should pay close attention to managing "supply pumping". As example, by either ensuring that the supply can sink current or by utilizing enough electrolytic energy storage to keep rail voltages within recommended operating range in all use situations. In a stereo/multichannel application it is recommended to alternate the phase of channels such that PSU rails are loaded as balanced as possible. However, this alone is not enough remedy to always avoid supply pumping and it is the responsibility of the system integrator to define and ensure adequate levels of caution.

4.1.2 Gate Drive Supply (VDR)

1ET6525SA requires an external supply for the gate drive circuitry. It is essential that the supply is designed as a floating rail, that must be referenced to -VP.

VDR directly feeds the low-side gate driver; the design utilizes boot-strap circuitry to create a rail relative to high-side driver.

4.1.3 OPAMPs Supply (+VOP, -VOP)

1ET6525SA requires an external ground-centered split-rail supply for the modulator and general analog low-power circuitry. There are no particular design constraints outside of normal audio design best-practice.

4.1.4 (optional) Digital Supply (VD)

The module includes a voltage regulator for the digital supply, sourced by +VOP and therefore does not require an external power supply for the digital section. To communicate with the module via I2C when the op amp supplies are powered down, VD can be connected to an external 5V supply that will supply the on-board microcontroller.

4.1.5 Power Supply Sequencing

1ET6525SA monitors all supplies with the exception of the optional VD supply and prevents operation unless all supply voltages are within preset safe thresholds.

4.2 Control Signals

4.2.1 PSUDIS & /AMPON

Signals share the same physical net and adapt function according to Operation mode (refer to section 5).

The net is tied directly to a microcontroller GPIO pin and has a 27kΩ pull-up to 5V.

4.2.2 SCL & /FATAL

Signals share the same physical net and adapt function according to Operation mode (refer to section 5).

The signal is connected to the collector of a transistor which has the emitter tied to a uC GPIO pin and the base tied permanently to 5V via a 3.3kΩ resistor.

As SCL, the transistor will level-shift the incoming signal to levels suitable for the uC.

As /FATAL, the transistor will pass output from the microcontroller and function as open-collector output.

4.2.3 SDA & READY

Signals share the same physical net and adapt function according to Operation mode (refer to section 5).

The net is tied directly to a microcontroller GPIO pin.

As SDA, the signal is a bi-directional (open-drain) I/O and complies with the general I2C specification in terms of levels and timing.

As READY, the signal is configured as CMOS-level compliant logic output.

4.3 Audio Inputs & Output

4.3.1 Audio Input (IN+, IN-)

1ET6525SA has a differential analog input.

The behavior of the input can be described as equivalent to a traditional differential op-amp configuration with gain and input resistance as listed in Table 4.

For best performance specs the overall amplifier gain is kept reasonably low. If desired, a separate gain stage can be implemented upstream to 1ET6525SA. It is up to the system integrator to specify the properties of any pre-gain/signal-conditioning circuitry as well as test how it affects the rest of the system.

Adjusting the 1ET6525SA input resistors voids all performance specifications and should therefore be avoided.

Amplifier clipping is a function of supply voltage (VP), amplifier gain and audio input voltage. As example, in nominal operating conditions (see Table 2) a balanced analog input of 10.8Vrms sine is required for the output to produce a signal with ~1% THD indicating the point where the amplifier is close to clipping.

4.3.2 Speaker Output (OUT+, OUT-)

1ET6525SA has a single-ended ground-centered speaker output.

The system integrator might notice that the OUT- terminal is connected to GND and be tempted to route the negative speaker terminal to GND elsewhere in the system. This, however, should be avoided as the internal feedback connections sense the voltage between OUT+ and OUT- terminals. Best performance is achieved by treating the speaker outputs as a balanced pair.

Bridging two 1ET6525SA modules may result in performance degradation as the circuit is not configured to sense the voltage differential that exists between the (now unused) OUT- terminals of the two 1ET6525SA designs. Bridging is therefore not recommended, and all operation and performance specs are void in this configuration. It should be noted that while the amplifier protection systems remain fully intact in a bridged configuration, it is not possible for the individual half-bridges (modules) to detect a DC across the speaker load (i.e. between two modules).

5 Operating Modes & Status Reporting

1ET6525SA can operate in two modes:

1. HW Mode: all control via pins (HW interface)
2. SW Mode: enables I2C control (I2C interface)

Modes are selected via resistor value programming, please see Table 8

5.1 Mode Selection (HS/ADDR Settings)

The programming resistor must be connected between the HS/ADDR pin and GND.
Setting of the HS/ADDR signal defines operation mode and I2C address per following table:

Mode	I2C Address	Resistor: HS/ADR to GND
Hardware Mode	-	∞ (not populated)
Software Mode	0x50	0
	0x51	1K9
	0x52	3K9
	0x53	6K8
	0x54	10K
	0x55	12K
	0x56	18K
	0x57	22K
	0x58	27K
	0x59	33K
	0x5A	47K
	0x5B	56K
	0x5C	82K
	0x5D	120K
	0x5E	190K
	0x5F	390K

*) Resistors must be 1% or better.

Table 8 Mode Selection via HS/ADDR

5.2 HW Modes

In HW Mode the channel controller monitors and operates all available circuits for environmental checks (Over/Under-voltage, Temperature) and all protection circuits (Current limiting, Overload protection, DC protection, Frequency protection and Bootstrap refresh).

Status and control information are accessible via three signals (nets):

NET	Signal	Rating	I/O	Description
J3,32	/AMPON	Table 2	I	Amplifier Disable – *pull low to enable Amp*
J3,25	READY		O	Amplifier Ready – "all good for operation" when high
J3,36	/FATAL		O	Amplifier "error/fail" – *signal goes low on error*

Table 9 Status/Control signals in HW Mode

5.3 SW Mode

The main feature of the SW Mode is access via I2C to a vast amount of status and control information.

I2C is accessed via SCL, SDA.

In addition to status/control information accessible via I2C, one hardwired output signal (PSUDIS) is available.

Pin	Signal	Rating	I/O	Description
J3,32	PSUDIS	Table 2	O	PSU off control signal
J3,35	SDA		I	I2C Data
J3,36	SCL		I	I2C clock

Table 10 Status/Control signals in SW Mode

5.3.1 PSUDIS (GPIO)

PSUDIS is essentially a GPIO which can be configured via the I2C register. Per default, GPIO is set to echo the AmpFail flag and is intended to be used to control the power supplies on and off.

It is possible to force the GPIO (i.e., SMPS_OFF) high or low via the I2C register – this enables control of the power supplies via the amplifier I2C interface.

GPIODir	DPIOVal	GPIOAmpFail	Description
0	0	0	GPIO is forced low
0	1	0	GPIO is forced high
1	x	0	Reserved
x	x	1	GPIO echoes the AmpFail flag (default)

Table 11 PSUDIS (GPIO) mapping

5.4 I2C Register Map

Reg	Name	Data type	R/W	Description
0x00	Channel count	High Nibble	R	1 = module has one active channels
	Product Type	Low Nibble	R	1 = amplifier module
0x01 0x02	Power	Integer	R	0x19 0x7D — 0x197D = 6525 (dec) = "65V, 25A" module
0x03	Version	High Nibble	R	Hardware revision number
	Revision	Low Nibble	R	Hardware sub-revision number
0x04 0x05	Serial	Integer		Serial number (convert hex to dec to get serial number)
0x06	Firmware	High Nibble	R	Firmware revision number
		Low Nibble	R	Firmware sub-revision number
0x07	Reserved	-	-	
0x08	Reserved	-	-	
0x09	Reserved	Bits 7-4	-	
	GPIOAmpFail	Bit 3	W	Set to make pin high when AmpFail is high, and Hi-Z otherwise
	GPIODir	Bit 2	W	Set low for using GPIO feature
	GPIOVal	Bit 1	W	GPIO pin value
	AmpEnable	Bit 0	W	Request to turn on amplifier
0x0A	Reserved	Bits 7-3	-	
	ICLIP	Bit 2	R	Flags that current limiting has happened since this flag was last read
	VCLIP	Bit 1	R	Flags that at clipping has happened at least once since this flag was last read
	AmpReady	Bit 0	R	Power stage is switching and passing signal
0x0B	Reserved	Bit 7	-	
	AmpFail	Bit 6	R	Flags that DC at the output persisted after turning the power stage off
	OverTemp	Bit 5	R	Temperature too high.
	MinVOPOver	Bit 4	R	Negative op-amp supply too high.
	PlusVOPOver	Bit 3	R	Positive op-amp supply too high.
	VDROver	Bit 2	R	VDR too high.
	MinHVOver	Bit 1	R	Negative high-voltage supply too high.
	PlusHVOver	Bit 0	R	Positive high-voltage supply too high.
0x0C	Reserved	Bits 7-6	-	
	UnderTemp	Bit 5	R	Temperature too low.
	MinVOPUnder	Bit 4	R	Negative op-amp supply too low.
	PlusVOPUnder	Bit 3	R	Positive op-amp supply too low.
	VDRUnder	Bit 2	R	VDR too low.
	MinHVUnder	Bit 1	R	Negative high-voltage supply too low.
	PlusHVUnder	Bit 0	R	Positive high-voltage supply too low.
0x0D	Reserved	Bits 7-2	-	
	OverloadError	Bit 1	R	Power stage is temporarily turned off after a sustained overcurrent event
	DCError	Bit 0	R	Power stage is temporarily turned off after DC was detected on the output.
0x0E	PlusVP	Unsigned short	R	Measured positive high-voltage rail in volts
0x0F	MinVP	Unsigned short	R	Measured negative high-voltage rail in volts
0x10	VDR	Unsigned short	R	Measured VDR in decivolts.
0x11	Temperature	Signed short	R	Measured temperature in °C
0x12	DC	Signed short	R	Measured output DC in volts
0x13 0x14	Fsw	Unsigned int	R	Measured switching frequency in units of 250Hz.
0x15	PlusVOP	Unsigned short	R	Measured positive op amp supply, in decivolts
0x16	MinVOP	Unsigned short	R	Measured negative op amp supply, in decivolts
0x17... 0x1F	Reserved	-	-	

Table 12 I2C Register Map

6 Protection System

1ET6525SA is protected from overload and failure by means of several protection circuits. All systems are continuously active while the amplifier is powered and operating.

6.1 Environmental checks

Environmental checks denote circuits that monitor operating conditions maintained or affected by external sources or influences such as power supply voltages and ambient/system temperatures.

Environmental checks are enabled in both HW Mode and SW Mode.

6.1.1 Over/Under-Voltage Protection, +VP, -VP, VDR, +VOP, -VOP

The high voltage supply rails (Power Stage Supply) must be within certain thresholds for safe operation. If supply levels are outside min-to-max thresholds denoted in table below the Amplifier power stage output is brought immediately into high-impedance state (HIZ).

In HW Mode an OVP/UVP condition asserts the READY signal low. It is recommended that the system host monitors this signal.

In SW Mode OVP/UVP states are reported in the I2C register with a great deal of associated information available, please refer to the I2C register map for details.

6.1.2 Temperature Protection, Backplate

1ET6525SA utilizes circuitry to monitor the temperature of the required aluminum back plate (used for cooling the FET's) and take appropriate action conditions are outside recommended operating range.

An OTP/UTP condition brings the amplifier output into high-impedance state (stop switching). Normal operation automatically resumes once temperatures return within the tolerable range and no involvement from user or system host controller is required.

In Hardware Mode an OTP/UTP condition asserts the READY signal low for as long as the temperature is out of tolerable range. It is recommended that the system host monitors this signal.

In Software Mode OTP/UTP status and actual measured temperature are reported in the I2C register, please refer to the register map for additional information.

6.2 Overcurrent Protection (OCP)

Each amplifier channel is protected against short- and long-term high-current overload.

A system monitors the output stage current and abruptly engages a *protection cycle* (*OCP cycle*) if a pre-set overcurrent threshold is exceeded. During a *protection cycle* the power stage output is flipped, i.e., if the overcurrent event concerns the high-side FET the half-bridge output will be force low, and reversely, if the overcurrent event concerns the low-side FET the half-bridge will be forced high. The duration of a *protection cycle* is approximately ~300nS or until the output current has decreased below a safe threshold. The combined behavior of the OCP circuit is comparable to a current-limiter function.

Extended current-limiting can result in triggering of the Overload Protection (refer to section 6.3).

Following a *protection cycle*, normal operation is automatically resumed and no involvement from user or system host controller is required.

OCP is enabled in all modes of operation (SW Mode, HW Mode).

OCP is reported in the I2C register (ICLIP) when operating in SW Mode.

6.3 Overload Protection (OLP)

To safeguard the Module against continuous operation at the OCP threshold (current-limiting) a circuit keeps track of OCP cycles as function of time. If the amplifier is running in current-limiting more than approximately 12% over time *an OLP mute cycle* is triggered. In events of continuous OCP the OLP triggers after approximately 10ms. During a *mute cycle* the output stage is disabled (left in high-impedance state) approximately 1 second.

Following a *mute cycle*, normal operation is automatically resumed and no involvement from user or system host controller is required.

OLP is enabled in all modes of operation (SW Mode, HW Mode).

OLP is reported in the I2C register (OverloadError) when operating in SW Mode.

6.4 DC Protection (DCP)

The amplifier audio signal channel is capable of passing DC signals, i.e., the audio channel does not include any form of low-cut (high-pass) filtering. To protect the speaker against potentially harmful DC signals 1ET6525SA includes a circuit that monitors the speaker output and disables the power stage should certain conditions be exceeded. The speaker output signal is low-pass filtered with a corner frequency below the audible range and if the filtered signal exceeds a preset threshold a DCP *mute cycle* is triggered (Table 4).

Following a *mute cycle*, normal operation is automatically resumed only if the DC is reduced within safe thresholds. If so, no involvement from user or system host controller is required. However, if DC persists at the end of the *mute cycle*, the power stage is latched off and will stay off until the user or system host controller takes deliberate action to restart operation.

DCP is enabled in SW Mode and HW Mode.

DCP-latch-off condition is reported in the I2C register (AmpFail) when operating in SW Mode. Note that a DCP *mute cycle* is not reported.

It is recommended to frequently poll the AmpFail flag and control the power supply accordingly. Alternatively, program the GPIO pin to output the state of AmpFail flag (default mode) and use that to shut down the power supply in case of a failure.

In HW Mode, DCP-latch-off condition asserts /FATAL signal low. It is recommended that the /FATAL signal is used to switch off the power supplies.

7 Mechanical Specifications & System Considerations

7.1 Module Dimensions

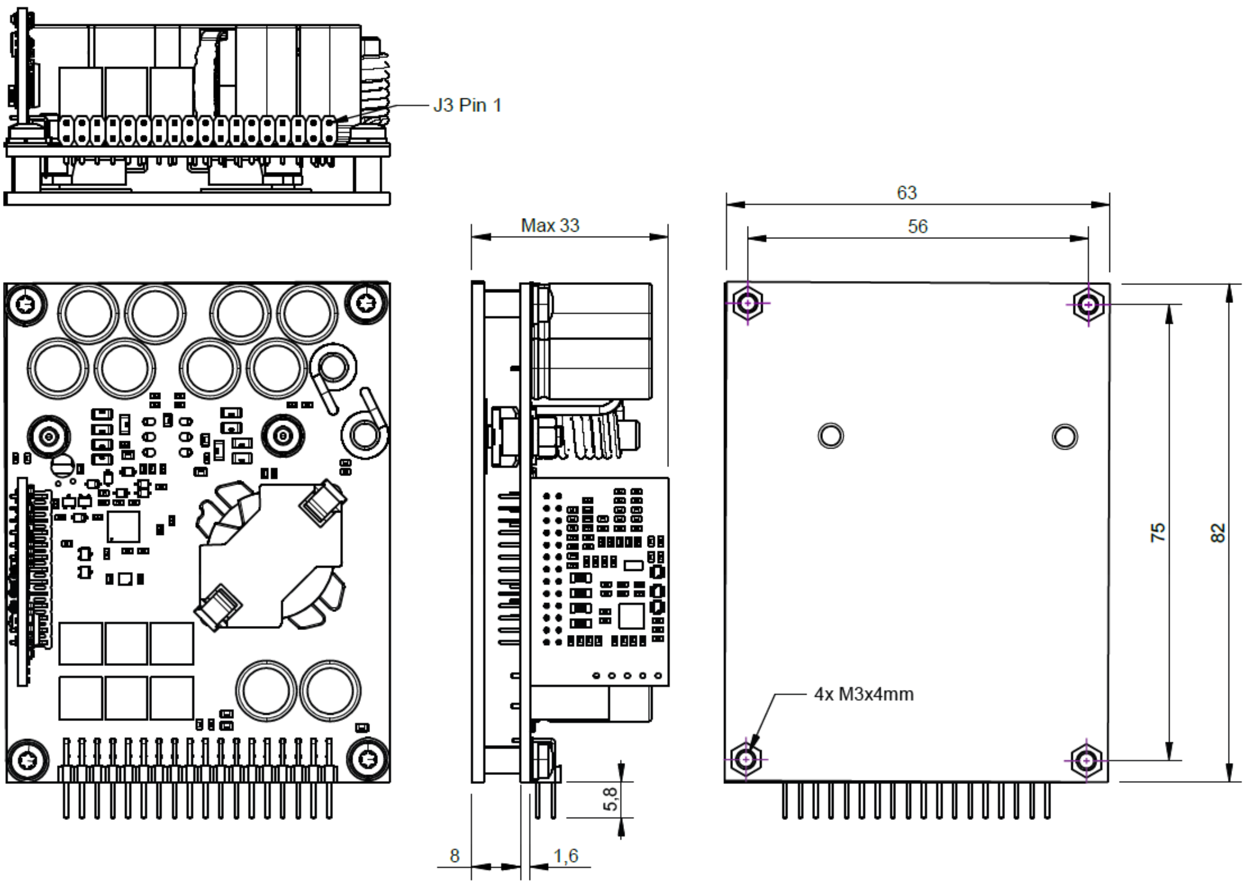


Figure 18 Dimensions

7.2 Thermal Requirements

While the 1ET6525SA boasts very low idle losses and high overall efficiency, proper cooling is crucial for maintaining sustained power delivery. To achieve the desired output power specifications, careful attention must be paid to the design of the thermal management system.

We recommend mounting the module on a heatsink, such as a well-designed aluminum chassis, and using a thermal interface material (e.g., thermal grease or pad) to optimize heat dissipation. This will ensure that the power stage operates efficiently while maintaining the desired ambient and heatsink temperatures.

7.3 Mechanical Requirements

Regarding the mechanical robustness of the final application, it is the responsibility of the system integrator to specify processes, materials, and locations for securing critical components, such as gluing, as needed. The system integrator must also prove and document both short- and long-term performance and reliability.

Ensuring the integrity of the mounting method and materials used to secure the module is crucial. We strongly recommend thoroughly testing the final product for robustness, including resistance to shock and vibration, to ensure reliable operation under all conditions.

7.4 Compliance Testing

1ET6525SA is designed with considerations for compliance of the end application. However, it is the responsibility of the system integrator to ensure any form of design-for-compliance and associated testing/certification which may be required.

8 Revision History

Rev	Date	Description	ID
(0.90)	2024-08	Prerelease version	SPO
(1.00)	2024-12	Final release	KNM

Table 13 Revision History

1 MODULE Use Restrictions and Warnings: 1.1 MODULES ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS. 1.2 User must read and apply the user guide and other available documentation provided by PURIFI ApS regarding the MODULE prior to handling or using the MODULE. 1.3 Safety-Related Warnings and Restrictions: 1.3.1 User shall operate the MODULE within PURIFI ApS's recommended specifications and environmental considerations stated in the specification or other available documentation provided by PURIFI APS, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the MODULE may cause personal injury or death, or property damage. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the MODULE and/or interface electronics. Please consult the MODULE documentation prior to connecting any load to the MODULE output. During normal operation, even with the inputs and outputs are kept within the specified allowable ranges, some circuit components may have elevated case temperatures. When working with the MODULE, please be aware that the MODULE may become very warm. If there is uncertainty as to the ratings and specifications, please contact PURIFI ApS prior to connecting interface electronics including input power and intended loads. 1.3.2 MODULEs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the MODULE by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the MODULE and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the MODULE by User or its employees, affiliates, contractors or designees. 1.4 User assumes all responsibility and liability to determine whether the MODULE is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the MODULE and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the MODULE consistent with all applicable international, federal, state, and local requirements.

2. Accuracy of Information: To the extent PURIFI ApS provides information on function of MODULEs, PURIFI ApS attempts to be as accurate as possible. However, PURIFI ApS does not warrant the accuracy of MODULE descriptions or other information on its websites as accurate, complete, reliable, current, or error-free.

3. Disclaimers: 3.1 EXCEPT AS SET FORTH ABOVE, MODULEs AND ANY WRITTEN MODULE MATERIALS PROVIDED WITH THE MODULE (AND THE DESIGN OF THE MODULE ITSELF) ARE PROVIDED "AS IS". PURIFI APS DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, REGARDING TO E.G. BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. 3.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE MODULE SET FORTH HEREIN, NOTHING IN THESE TERMS AND CONDITIONS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF PURIFI APS, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE MODULE IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT MADE, CONCEIVED OR ACQUIRED PRIOR TO OR AFTER DELIVERY OF THE MODULE.

4. USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS. USER WILL DEFEND, INDEMNIFY AND HOLD PURIFI APS, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE MODULE THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR LAW OF TORT, CONTRACT OR ANY OTHER LAW, AND EVEN IF THE MODULE FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

5. Limitations on Damages and Liability: 5.1 General Limitations. IN NO EVENT SHALL PURIFI APS BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS AND CONDITIONS OR THE USE OF THE MODULES PROVIDED HEREUNDER, REGARDLESS OF WHETHER PURIFI APS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST PURIFI ApS MORE THAN ONE YEAR AFTER THE RELATED INCIDENCE HAS OCCURRED. 5.2 Specific Limitations. IN NO EVENT SHALL PURIFI APS'S AGGREGATE LIABILITY FROM ANY WARRANTY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS AND CONDITIONS, OR ANY USE OF ANY PURIFI APS MODULE PROVIDED HEREUNDER, EXCEED THE TOTAL AMOUNT PAID TO PURIFI APS FOR THE PARTICULAR UNITS SOLD UNDER THESE TERMS AND CONDITIONS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM AGAINST THE PARTICULAR UNITS SOLD TO USER UNDER THESE TERMS AND CONDITIONS SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

6. Governing Law: These terms and conditions shall be governed by and interpreted in accordance with the laws of Denmark, excluding Denmark's conflict-of-law rules, leading to the use of other law than the laws of Denmark. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within the courts of Denmark and consents to venue in Copenhagen, Denmark. Notwithstanding the foregoing, any judgment may be enforced in Danish court, and PURIFI ApS may seek injunctive relief in Denmark or foreign countries.